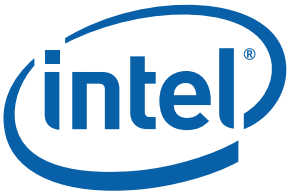

Intel® C102/C104 Scalable Memory Buffer

Datasheet

February 2014

Reference Number: 330032-001

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Revision History

Revision Number	Description	Date
001	• Initial Revision	February 2014

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1 Introduction

1.1 Document Scope

This specification introduces the interfaces, features, electrical and register specifications of the Intel® C102/C104 Scalable Memory Buffer. Intel® C102 Scalable Memory Buffer supports up to two DIMMs per DDR bus. Intel® C104 Scalable Memory Buffer supports up to three DIMMs per DDR bus.

1.2 Intel® C102/C104 Scalable Memory Buffer Overview

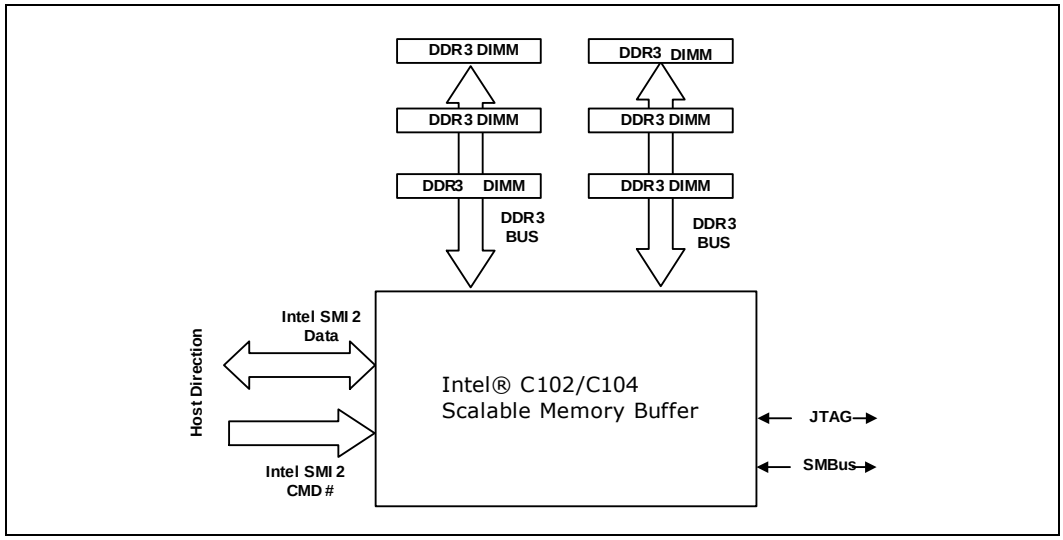
Intel® C102/C104 Scalable Memory Buffer supports DDR3 SDRAM main memory. The primary interface to the host memory controller is an Intel® Scalable Memory Interconnect 2 (Intel® SMI 2) channel.

Intel® C102/C104 Scalable Memory Buffer is responsible for handling Intel® SMI 2 channel and memory requests to and from the local DIMM. All memory control for the DRAM resides in the host, that is, integrated memory controller in the CPU, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management.

1.3 Intel® C102/C104 Scalable Memory Buffer Interfaces and Features

Figure 1-1 illustrates the Intel® C102/C104 Scalable Memory Buffer and its interfaces. They consist of one Intel® SMI 2 link, two DDR3 buses, a JTAG interface, and an SMBus interface.

Figure 1-1. Intel® C102/C104 Scalable Memory Buffer Interfaces



1.3.1 Intel® Scalable Memory Interconnect 2 (Intel® SMI 2)

1.3.1.1 Intel® SMI 2 Signals List

Table 1-1. Intel® SMI 2 Signal List

Group Name	Signal Name	# of Signals	# of Pins
Data Bus		**81**	**90**
Data bits	VMSEDQ[63:0]	64	64
ECC Check bits	VMSEDQ[71:64]	8	8
Strobes	VMSEDQSP[8:0],VMSEDQSN[8:0]	9	18
Command Bus		**17**	**17**
Command bits	VMSECMD_N[16:0]	17	17
Clocks		**2**	**4**
VMSE Clock	VMSECKP, VMSECKN	1	2
Reference Clock	REFCK100P, REFCK100N	1	2
Misc. Signals		**1**	**1**
Error	VMSE_ERR_N	1	1
TOTAL		**101**	**112**

The Intel® SMI 2 channel consists of a CMD# bus (Command/Address), a data bus, an error signal, and reference clock signals.

The CMD# bus is a 17 bit unidirectional bus from the host to the Intel® C102/C104 Scalable Memory Buffer, and carries DRAM command, address, and control information, as well as non-DRAM commands to the Intel® C102/C104 Scalable Memory Buffer. One differential strobe pair, VMSECKP/VMSECKN is used for clocking for the CMD# bus.

The data bus is a 72 bit wide bidirectional bus which carries DRAM read and write data, as well as Intel® C102/C104 Scalable Memory Buffer configuration register read data. The 72 bits are grouped into 9 groups of 8 bits, with each group containing a differential strobe pair.

The Error signal is a unidirectional signal from the Intel® C102/C104 Scalable Memory Buffer to the host. It is asynchronous, having no strobe associated with it.

1.3.1.2 Intel® SMI 2 Modes of Operation

The Intel® SMI 2 channel can be operated in either

- 2:1 Independent Channel Mode OR
- 1:1 Sub-Channel Lockstep Mode

1.3.1.2.1 2:1 Independent Channel Mode

In the 2:1 mode, Independent Channel operation, the Intel® SMI 2 channel operates at double the data rate of the back side DRAM busses. This allows both busses to operate at full bandwidth simultaneously, and also allows commands to be sent to both busses independently and simultaneously at the full command rate. Intel® C102/C104 Scalable Memory Buffer supports 2:1 Independent Channel Operation at 2133 and 2667 MT/s.

1.3.1.2.2 1:1 Sub-channel Lockstep Mode

In Sub-Channel lockstep, one command sent on the Intel® SMI 2 CMD# bus targets two DIMMs, one on each DRAM bus behind the Intel® C102/C104 Scalable Memory Buffer. The read or write commands are issued simultaneously to the DIMMs, and the Intel® C102/C104 Scalable Memory Buffer interleaves the data on the Intel® SMI 2 data bus.

Intel® C102/C104 Scalable Memory Buffer supports 1:1 Sub-Channel Lockstep Operation at 1066, 1333, 1600 MT/s.

1.3.1.3 Half Width Support

Intel® C102/C104 Scalable Memory Buffer supports Half width mode which allows the Intel® SMI 2 channel to continue to operate at a reduced bandwidth when there is a single failure on any data lane failure, and 9 out of 10 of the strobe pairs.

1.3.1.4 Hot Insertion and Removal

Intel® C102/C104 Scalable Memory Buffer does not support hot insertion or removal of individual DIMMs. Hot insertion and removal at the Intel SMI 2 channel interface can be accomplished.

Intel® C102/C104 Scalable Memory Buffer does not support insertion or removal while power is applied to the Intel® C102/C104 Scalable Memory Buffer component. Intel SMI 2 transmitters of the host must be disabled while the Intel® C102/C104 Scalable Memory Buffer component is hot inserted or removed.

1.3.2 DDR3

Intel® C102/C104 Scalable Memory Buffer provides two DDR3 interfaces. Each interface provides the following functionality.

- DDR3 protocol and signalling.
- Support for RDIMM, LR DIMM, Low Voltage DIMM.
  - — Both DDR busses must operate at the same voltage.
  - — DDR3 Low Voltage DIMMs are supported at 1.35 V.
- Up to eight logical ranks per DDR bus (sixteen per Intel® C102/C104 Scalable Memory Buffer)
- 1066, 1333, 1600 MT/s signaling.
  - — Both DDR busses must operate at the same frequency.
  - — Not all DIMM types and organizations are supported at all frequencies.
- Single Rank x4, Dual Rank x4, Quad Rank x4, Single Rank x8, Dual Rank x8, Quad Rank x8.
- 4 GB, 8 GB, 16 GB, 32 GB RDIMM and LR DIMM.
- 16 GB, 32 GB, 64 GB LR DIMM.
- Physical Device Technology DRAM: 2Gb, 4Gb.
- Logical Device Technology (for LR DIMM with Rank Multiplication):2 Gb, 4 Gb, 8 Gb, 16 Gb, 32 Gb, 64 Gb.
- In 2:1 Independent Channel Mode, DIMMs with independent device configurations are supported.
  - — DIMMs with different numbers of row, column, bank and ranks can be mixed.

  - DIMMs with different device sizes can be mixed.
  - DIMMs with x4 and x8 widths can be mixed.
- In 2:1 Independent Channel Mode, DDR busses may contain different number of DIMMs, zero through three.
- In Sub-Channel lockstep mode, DIMM sizes, rows, columns, and ranks must be the same across lockstepped pairs of DIMMs.
- DIMM types RDIMM or LR DIMM can not be mixed. In other words, Intel® C102/C104 Scalable Memory Buffer does not support RDIMM on one DDR bus and LR DIMM on the other, or mixed RDIMM and LR DIMM on the same bus.
- Cmd/Addr parity generation and error logging.
- Support for 1n/2n/3n timings
- No support for non-zero values of Additive Latency (AL)
- No support for Data Mask functionality.
- No support for non-ECC DIMMs.
- No support for S3.
- No support for burst on the fly.

1.3.3 SMBus

- Intel® C102/C104 Scalable Memory Buffer supports SMbus slave interface at 100 KHz. This provides access to all configuration and status registers out of band.

The SMBus slave interface is compliant with the *System Management Bus (SMBus) Specification*. The principal requirement from the SMBus 2.0 specification is support of the "high power" bus electrical specifications described in the layer 1 (Physical layer) chapter.

Intel® C102/C104 Scalable Memory Buffer supports the SMBus 2.0 layer 1 protocol, but does not support the full 3.3 V signal swing. The Intel® C102/C104 Scalable Memory Buffer SMBus interfaces operate at core digital voltage, and a converter external to Intel® C102/C104 Scalable Memory Buffer is required to interface to the full 3.3 V SMBus.

For the simple register access requirements of Intel® SMI 2, no layer 2 (Link layer) or layer 3 (Network layer) extensions provided by the 2.0 specification are used. In particular, there is no support for Address Resolution Protocol (ARP) since Intel® C102/C104 Scalable Memory Buffer is using fixed addresses.

Intel® C102/C104 Scalable Memory Buffer does not clock stretch on read and write transactions. Intel® C102/C104 Scalable Memory Buffer does not master SMBus transactions.

1.3.4 JTAG

Intel® C102/C104 Scalable Memory Buffer implements a JTAG (Joint Test Action Group) TAP controller as specified by IEEE 1149.1.The JTAG port is used for debugging silicon and to provide boundary scan for board testing. It is not supported for use during normal system operation. During system operation, TRST must be held low.

1.3.5 MemBIST

Intel® C102/C104 Scalable Memory Buffer supports memory built in self test (MemBIST) for memory initialization during system boot up and for testing the installed memory and Intel® C102/C104 Scalable Memory Buffer-to-DRAM interface.

1.3.6 Debug and Observability

Intel® C102/C104 Scalable Memory Buffer can be configured to provide an interface to a Logic Analyzer to enable Intel® SMI 2 channel observability.

1.4 References

This revision of Intel® C102/C104 Scalable Memory Buffer Specification is consistent with the following document revisions when they are referenced elsewhere in this specification:

Document	Revision
JESD79-3 DDR3 SDRAM Specification	July 2010
JESD82 LRDIMM Specification	
PCI Local Bus Specification	2.2
System Management Bus (SMBus) Specification	2.0
IEEE 1149.1a-1993 (JTAG)	
Registering Clock Driver with Parity for DDR3 RDIMM Applications	3/12/2008

1.5 List of Terms and Abbreviations

Term	Definition
VMSE	Voltage Mode Single Ended, also referred as Intel SMI2.
DDR	Double Data Rate (SDRAM)
DDR3	Double Data Rate - Third Generation
DDR Bus	A DDR Bus consists of a data bus with 72 bits of data and an ADDR/DDR Data bus A DDR data bus consists of 72 bits of data, divided into 18 data groups. DDR Data group Each data group consists of 4 data signals and a differential strobe pair
DRAM Page	The DRAM cells selected by the Row Address
DRAM	Dynamic Random Access Memory
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socket substrate.
ECC	Error Correction Code. For Intel® C102/C104 Scalable Memory Buffer, this is a chip disable code.
Intel® SMI 2	Intel® Scalable Memory Interconnect 2. This may be also referred to as VMSE.
LA	Logic Analyzer
LAI	Logic Analyzer Interface
CFIO	Configurable Input Output

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2 Signal List

2.1 Conventions

The terms *assertion* and *de-assertion* are used extensively when describing signals, to avoid confusion when working with a mix of active-high and active-low signals. The term *assert*, or *assertion*, indicates that the signal is active, independent of whether the active level is represented by a high or low voltage. The term *de-assert*, or *de-assertion*, indicates that the signal is inactive.

Signal names may or may not use the suffix "_N". The "_N" suffix indicates that the active, or asserted state occurs when the signal is at a low voltage level. When the "_N" suffix is not present in the signal name the signal is asserted when at the high voltage level. **TRST_N** is an example of a signal that is asserted when at the low voltage level.

Differential pairs include "P" or "N" in the individual signal name to indicate the "positive" (P) signal in the pair or the "negative" (N) signal in the pair. **REFCK100P and REFCK100N** is an example of such a pair. When referring to the logic encoded by the differential pair of signals, sometimes the P/N notation will be dropped, e.g. **REFCK100**.

Curly-bracketed numerical indices, for example, "{0/1}", represent DDR bus numbers (e.g., **DDR{0/1}RAS_N**). Square-bracketed numerical indices, for example, "[3:0]" represent functionally similar but logically distinct bus signals; each signal provides an independent control, and may or may not be asserted at the same time as the other signals in the grouping. **DDR{0/1}CKE[5:0]** and **DDR{0/1}MA[15:0]** are examples.

Typical frequencies of operation for the fastest operating modes are indicated. Test guard bands are not included. No frequency is mentioned for asynchronous or analog signals.

Table 2-1 summarizes the signal naming conventions used in this document.

Table 2-1. Signal Naming Conventions

Convention	Expands to
RR{0/1/2}XX	Expands to: RR0XX, RR1XX, and RR2XX. This denotes similar signals on separate busses.
RR[2:0]	Expands to: RR[2], RR[1], and RR[0]. This denotes a bus.
RR_N or RR_N[2:0]	Denotes an active low signal or bus.
RRN and RRP	Denotes a differential pair.

2.2 Intel® C102/C104 Scalable Memory Buffer Component Pin Description List

Table 2-2. Intel® C102/C104 Scalable Memory Buffer Signal List (Sheet 1 of 4)

Signal	Signal Type	Description
Intel® SMI 2 Channel Interface		
VMSEDQ[63:0]	VMSE I/O	Intel® SMI 2 Data
VMSEDQ[71:64]	VMSE I/O	Intel® SMI 2 ECC Check bits
VMSEDQSP[8:0]	VMSE I/O Differential	Intel® SMI 2 Data Strobes
VMSEDQSN[8:0]	VMSE I/O Differential	Intel® SMI 2 Data Strobe Complements
VMSECMD_N[16:0]	VMSE Input	Intel® SMI 2 Command
VMSECKP	VMSE Input Differential	Intel® SMI 2 Command Clock
VMSECKN	VMSE Input Differential	Intel® SMI 2 Command Clock Complement
VMSE_ERR_N	VMSE Output	Intel® SMI 2 Asynchronous Error Signal
Intel® SMI 2 Compensation/Debug/Reg		
VMSE_CRES_P	VMSE Ref Res	cres_p and cres_n connect to opposite terminals of an external resistor, 35 ohm precision (±1% or better), for the COMP circuit.
VMSE_CRES_N	VMSE Ref Res	
VMSE_REXT	VMSE Ref Res	on the board connects to a 1 kΩ precision resistor ±1% to VSS.
DDR busses 0/1		
DDR{0/1}DQ[63:0]	DDR I/O	**DDR Data**
DDR{0/1}CB[7:0]	DDR I/O	**DDR Check bits**
DDR{0/1}DQSP[7:0]	DDR I/O Differential	**DDR Data Strobe:** x8 data strobes.
DDR{0/1}DQSN[7:0]	DDR I/O Differential	**DDR Data Strobe Complement:** x8 data strobe.
DDR{0/1}DQSP[8]	DDR I/O Differential	**DDR Check-bit Strobe:** x8 check-bit strobes.
DDR{0/1}DQSN[8]	DDR I/O Differential	**DDR Check-bit Strobe Complement: x8** check-bit strobe.
DDR{0/1}DQSP[16:9]	DDR I/O Differential	**DDR Data Strobe:** data strobes for x4 devices.Not used for x8 devices.
DDR{0/1}DQSN[16:9]	DDR I/O Differential	**DDR Data Strobe Complement:** data strobe complements for x4 devices. Not used for x8 devices.
DDR{0/1}DQSP[17]	DDR I/O Differential	**DDR Check-bit Strobe:** check-bit strobe for x4 devices.Not used for x8 devices.
DDR{0/1}DQSN[17]	DDR I/O Differential	**DDR Check-bit Strobe Complement:** check-bit strobe complements for x4 devices. Not used for x8 devices.
DDR{0/1}MA[15:0]	DDR I/O	**Address:** Used for providing multiplexed row and column address to RDIMM.
DDR{0/1}BA[2:0]	DDR Output	**Bank Active:** Used to select the bank within a rank.
DDR{0/1}ACT_N	DDR Input/Output	DDR3: Input Pin; Connects to parity error signal from the DIMM (slot 2).
DDR{0/1}RAS_N	DDR Output	Row Address Strobe: For DDR3, used with CS_N, CAS_N, and WE_N to specify the DDR command.

Table 2-2. Intel® C102/C104 Scalable Memory Buffer Signal List (Sheet 2 of 4)

Signal	Signal Type	Description
DDR{0/1}CAS_N	DDR Output	Column Address Strobe: For DDR3, used with CS_N, RAS_N, and WE_N to specify the DDR command.
DDR{0/1}WE_N	DDR Output	Write Enable: For DDR3, used with CS_N, CAS_N, and RAS_N to specify the DDR command.
DDR{0/1}CS_N[9:0]	DDR Output	DDR Chip Select: For DDR3, used with CAS_N, RAS_N, and WE_N to specify the DDR command. ***Note:*** For DDR3 LR DIMM, A[17:16] can be multiplexed onto CS_N[9:8], CS_N[7:6] and CS_N[3:2].
DDR{0/1}C0	DDR I/O	DDR3: Input Pin; Connects to parity error signal from the DIMM (slot 1).
DDR{0/1}CKE[5:0]	DDR Output	**Clock Enable:** DIMM Clock enable.
DDR{0/1}ODT[5:0]	DDR Output	**DIMM On-Die-Termination:** Dynamic ODT enables. ***Note:*** For DDR3 LR DIMM, A18 can be multiplexed onto ODT1, ODT3, and/or ODT5 instead of ODT.
DDR{0/1}PAR	DDR Output	**Parity bit protecting MA, BA, RAS_N, CAS_N, WE_N**.
DDR{0/1}ERR_N	DDR Input	**Wired OR Parity error detected signal from DIMMs**. No external pull-up required, since there is a 50 ohm internal pull-up on this signal.
DDR{0/1}RESET_N	DDR Output	**DIMM Reset**. This signals drives the RESET_N inputs of the DIMMs. RESET_N is asynchronous
DDR{0/1}CKP[3:0]	DDR Output	**Clock:** Clocks to DIMMs.
DDR{0/1}CKN[3:0]	DDR Output	**Clock Complement:** Clocks to DIMMs.
DDR Compensation/Debug/Reg		
DDR_COMP	DDR Analog	Analog Compensation. On the board connects to 100 ohm precision resistor (±1%) to VSS.
DDR{0/1}TXVREF	DDR Analog	Vref for DIMM DQ/Command and Address. Intel® C102/C104 Scalable Memory Buffer does not support routing DDR{0/1}TXVREF signal to the DIMMs.
Reference Clocking		
REFCK100P	Reference Clock Input	Intel® C102/C104 Scalable Memory Buffer Clock: This is one of the two differential reference clock inputs to the Phase Locked Loop in the Intel® C102/C104 Scalable Memory Buffer core.
REFCK100N	Reference Clock Input	Intel® C102/C104 Scalable Memory Buffer Clock Complement: This is the other differential reference clock input to the Phase Locked Loop in the Intel® C102/C104 Scalable Memory Buffer core.
System Management		
SCL	CFIO Input	SMBus Clock. Needs onboard level shifters to convert 3.3 V signal to 1 V. vih=vccdcore*0.7 vil=vccdcore*0.3

Table 2-2. Intel® C102/C104 Scalable Memory Buffer Signal List (Sheet 3 of 4)

Signal	Signal Type	Description
SDA	Open Drain CFIO I/O	SMBus Address/Data. The SDA signal needs a 1Kohm pullup resistor connected to vcccore (1.0 V). Needs onboard level shifters to convert 3.3 V signal to 1 V. vih=vccdcore*0.7 vil=vccdcore*0.3 voh=vccdcore vol=vccdcore*0.2
SA0	CFIO Input	SMBus Select ID. vih=vccdcore*0.7 vil=vccdcore*0.3
Reset		
VCCAIO_PWRGOOD	Schmitt Input	Power Good indication for DDR IO voltage. Should be 1.0 V compatible (vccdcore_1p0) voltage rail. Vih=vcc*0.75; Vil= vcc*0.25
VCCD_PWRGOOD	Schmitt Input	Power Good indication for VCC digital voltage. Should be 1.0 V compatible (vccdcore_1p0) voltage rail. Vih=vcc*0.75; Vil= vcc*0.25
RST_N	Schmitt Input	Asynchronous Reset. Should be 1.0 V compatible (vccdcore_1p0) voltage rail. Vih=vcc*0.75; Vil= vcc*0.25
Logic Analyzer		
TRIG[2:0]	CMOS Output	**Logic Analyzer Triggers:** voh=vccdcore vol=vccdcore*0.2
Test Access Port (JTAG)		
TCK	CFIO Input weak pull-down 2K ohm.	**JTAG Test Clock:** Clock input used to drive Test Access Port (TAP) state machine during test and debugging. This input may change asynchronous to REFCK100. vih=vccdcore*0.7 vil=vccdcore*0.3
TDI	CFIO Input weak pull up 2K ohm.	**JTAG Test Data In:** Data input for test mode. Used to serially shift data and instructions into TAP. vih=vccdcore*0.7 vil=vccdcore*0.3
TDO	TDO (Open Drain CFIO Output)	**JTAG Test Data Out:** Data: Data output for test mode. Used to serially shift data out of the device. This signal needs a 50 ohm pull-up resistor to VCCcore (1.0V) vih=vccdcore*0.7 vil=vccdcore*0.3 voh=vccdcore vol=vccdcore*0.2
TMS	CFIO Input weak Pull up 2K ohm.	**JTAG Test Mode Select:** This signal is used to control the state of the TAP controller. vih=vccdcore*0.7 vil=vccdcore*0.3
TRST_N	CFIO Input Weak pull up 2K ohm	**JTAG Test Reset:** This signal resets the TAP controller logic. It should be pulled down unless TCK is active. This input may change asynchronous to REFCK100. vih=vccdcore*0.7 vil=vccdcore*0.3

Table 2-2. Intel® C102/C104 Scalable Memory Buffer Signal List (Sheet 4 of 4)

Signal	Signal Type	Description
Thermal Sensor		
BIREF_NPAD	INPUT	BIREF_NPAD needs to be connected to VSS via a 8.06 K ohm, 1%, 1/16 W.
Other Pins		
RSVD (multiple pins)	NC	NC and Reserved pins in the ball out must be floated.

Table 2-3. Intel® C102/C104 Scalable Memory Buffer Power Pins

Power Supplies	Nominal Voltage	
VCCDCORE_1P0 VCCDVMSEIO_1P0	1.0	Digital supply for core, shorted on die to DDR, miscellaneous, and thermal sensor.
VCCADDRIO_1P5	1.5, 1.35	DDR IO source. DDR3 @ 1.5 V, LVDDR@1.35 V.
VCCADDRDLL_1P5 VCCAVMSEPLL_1P5 VCCAMISCTS_1P5	1.5	DDR DLL analog rail, powers the DDR VRMs PLL supply, powers PLL VRM. Thermal Sensor Supply
VCCAVMSEIO_1P35	1.35	Intel® SMI 2 IO Source
VSS (multiple pins)		Ground

2.3 Intel® C102/C104 Scalable Memory Buffer Ball List

Table 2-4 is a listing of Ball list ordered by row number (LHS) and by signal groups (RHS).

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 1 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
0	1	1	AC38	----	1	R27	NC
1	1	2	AC37	VSS	2	P25	NC
2	1	3	AC36	VSS	3	T25	BIREF_NPAD
3	1	4	AC35	VSS	4	T24	NC
4	1	5	AC34	VSS	5	U20	NC
5	1	6	AC33	DDR0ODT[3]	6	T19	DDR_COMP
6	1	7	AC32	DDR0ODT[2]	7	AA16	DDR0ACT_N
7	1	8	AC31	DDR0CS_N[2]	8	AB22	DDR0BA[0]
8	1	9	AC30	DDR0ODT[1]	9	AC26	DDR0BA[1]
9	1	10	AC29	DDR0CS_N[0]	10	AC16	DDR0BA[2]
10	1	11	AC28	DDR0CKN[2]	11	AA17	DDR0C0
11	1	12	AC27	DDR0CKP[2]	12	AC21	DDR0CAS_N
12	1	13	AC26	DDR0BA[1]	13	V4	DDR0CB[0]
13	1	14	AC25	DDR0CKN[0]	14	W4	DDR0CB[1]
14	1	15	AC24	VCCADDRIO_1P5	15	AA4	DDR0CB[2]
15	1	16	AC23	DDR0PAR	16	Y4	DDR0CB[3]
16	1	17	AC22	DDR0MA[2]	17	V5	DDR0CB[4]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 2 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
17	1	18	AC21	DDR0CAS_N	18	W5	DDR0CB[5]
18	1	19	AC20	DDR0MA[3]	19	AA3	DDR0CB[6]
19	1	20	AC19	VCCADDRIO_1P5	20	AB4	DDR0CB[7]
20	1	21	AC18	DDR0MA[7]	21	AB13	DDR0CKE[0]
21	1	22	AC17	DDR0MA[9]	22	AB14	DDR0CKE[1]
22	1	23	AC16	DDR0BA[2]	23	AC13	DDR0CKE[2]
23	1	24	AC15	DDR0MA[15]	24	AA13	DDR0CKE[3]
24	1	25	AC14	VCCADDRIO_1P5	25	Y14	DDR0CKE[4]
25	1	26	AC13	DDR0CKE[2]	26	Y15	DDR0CKE[5]
26	1	27	AC12	VSS	27	AC25	DDR0CKN[0]
27	1	28	AC11	DDR1CB[3]	28	AA28	DDR0CKN[1]
28	1	29	AC10	DDR1CB[7]	29	AC28	DDR0CKN[2]
29	1	30	AC9	DDR1DQSP[8]	30	AB28	DDR0CKN[3]
30	1	31	AC8	DDR1DQSN[17]	31	AB25	DDR0CKP[0]
31	1	32	AC7	DDR1CB[1]	32	AA27	DDR0CKP[1]
32	1	33	AC6	DDR1CB[5]	33	AC27	DDR0CKP[2]
33	1	34	AC5	VSS	34	AB27	DDR0CKP[3]
34	1	35	AC4	VSS	35	AC29	DDR0CS_N[0]
35	1	36	AC3	VSS	36	AB30	DDR0CS_N[1]
36	1	37	AC2	VSS	37	AC31	DDR0CS_N[2]
37	1	38	AC1	----	38	AA31	DDR0CS_N[3]
38	2	1	AB38	VSS	39	AB32	DDR0CS_N[4]
39	2	2	AB37	VSS	40	AA32	DDR0CS_N[5]
40	2	3	AB36	VSS	41	AA33	DDR0CS_N[6]
41	2	4	AB35	VSS	42	AB33	DDR0CS_N[7]
42	2	5	AB34	VSS	43	W13	DDR0CS_N[8]
43	2	6	AB33	DDR0CS_N[7]	44	Y13	DDR0CS_N[9]
44	2	7	AB32	DDR0CS_N[4]	45	C3	DDR0DQ[0]
45	2	8	AB31	VCCADDRIO_1P5	46	D4	DDR0DQ[1]
46	2	9	AB30	DDR0CS_N[1]	47	K2	DDR0DQ[10]
47	2	10	AB29	VCCADDRIO_1P5	48	K1	DDR0DQ[11]
48	2	11	AB28	DDR0CKN[3]	49	D2	DDR0DQ[12]
49	2	12	AB27	DDR0CKP[3]	50	E2	DDR0DQ[13]
50	2	13	AB26	VCCADDRIO_1P5	51	J2	DDR0DQ[14]
51	2	14	AB25	DDR0CKP[0]	52	J1	DDR0DQ[15]
52	2	15	AB24	DDR0MA[10]	53	M5	DDR0DQ[16]
53	2	16	AB23	DDR0MA[0]	54	M4	DDR0DQ[17]
54	2	17	AB22	DDR0BA[0]	55	T4	DDR0DQ[18]
55	2	18	AB21	VCCADDRIO_1P5	56	T5	DDR0DQ[19]
56	2	19	AB20	DDR0MA[4]	57	H5	DDR0DQ[2]
57	2	20	AB19	DDR0MA[6]	58	L5	DDR0DQ[20]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 3 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
58	2	21	AB18	DDR0MA[8]	59	L4	DDR0DQ[21]
59	2	22	AB17	DDR0MA[11]	60	R4	DDR0DQ[22]
60	2	23	AB16	VCCADDRIO_1P5	61	R5	DDR0DQ[23]
61	2	24	AB15	DDR0MA[14]	62	N2	DDR0DQ[24]
62	2	25	AB14	DDR0CKE[1]	63	N1	DDR0DQ[25]
63	2	26	AB13	DDR0CKE[0]	64	U2	DDR0DQ[26]
64	2	27	AB12	VSS	65	U1	DDR0DQ[27]
65	2	28	AB11	DDR1CB[2]	66	M2	DDR0DQ[28]
66	2	29	AB10	DDR1CB[6]	67	M1	DDR0DQ[29]
67	2	30	AB9	DDR1DQSN[8]	68	J5	DDR0DQ[3]
68	2	31	AB8	DDR1DQSP[17]	69	T2	DDR0DQ[30]
69	2	32	AB7	DDR1CB[0]	70	T1	DDR0DQ[31]
70	2	33	AB6	DDR1CB[4]	71	AA36	DDR0DQ[32]
71	2	34	AB5	VSS	72	Y36	DDR0DQ[33]
72	2	35	AB4	DDR0CB[7]	73	W34	DDR0DQ[34]
73	2	36	AB3	VSS	74	V34	DDR0DQ[35]
74	2	37	AB2	VSS	75	Y35	DDR0DQ[36]
75	2	38	AB1	VSS	76	AA35	DDR0DQ[37]
76	3	1	AA38	VSS	77	V36	DDR0DQ[38]
77	3	2	AA37	VSS	78	V35	DDR0DQ[39]
78	3	3	AA36	DDR0DQ[32]	79	B4	DDR0DQ[4]
79	3	4	AA35	DDR0DQ[37]	80	T38	DDR0DQ[40]
80	3	5	AA34	VSS	81	T37	DDR0DQ[41]
81	3	6	AA33	DDR0CS_N[6]	82	M38	DDR0DQ[42]
82	3	7	AA32	DDR0CS_N[5]	83	M37	DDR0DQ[43]
83	3	8	AA31	DDR0CS_N[3]	84	U38	DDR0DQ[44]
84	3	9	AA30	DDR0ODT[0]	85	U37	DDR0DQ[45]
85	3	10	AA29	VCCADDRIO_1P5	86	N38	DDR0DQ[46]
86	3	11	AA28	DDR0CKN[1]	87	N37	DDR0DQ[47]
87	3	12	AA27	DDR0CKP[1]	88	J38	DDR0DQ[48]
88	3	13	AA26	RSVD	89	J37	DDR0DQ[49]
89	3	14	AA25	RSVD	90	C4	DDR0DQ[5]
90	3	15	AA24	VCCADDRIO_1P5	91	E37	DDR0DQ[50]
91	3	16	AA23	DDR0RAS_N	92	D37	DDR0DQ[51]
92	3	17	AA22	DDR0WE_N	93	K38	DDR0DQ[52]
93	3	18	AA21	DDR0MA[13]	94	K37	DDR0DQ[53]
94	3	19	AA20	DDR0MA[1]	95	F38	DDR0DQ[54]
95	3	20	AA19	VCCADDRIO_1P5	96	F37	DDR0DQ[55]
96	3	21	AA18	DDR0MA[5]	97	J35	DDR0DQ[56]
97	3	22	AA17	DDR0C0	98	H35	DDR0DQ[57]
98	3	23	AA16	DDR0ACT_N	99	E34	DDR0DQ[58]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 4 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
99	3	24	AA15	DDR0MA[12]	100	D34	DDR0DQ[59]
100	3	25	AA14	VCCADDRIO_1P5	101	H4	DDR0DQ[6]
101	3	26	AA13	DDR0CKE[3]	102	J34	DDR0DQ[60]
102	3	27	AA12	DDR0RESET_N	103	H34	DDR0DQ[61]
103	3	28	AA11	VSS	104	E35	DDR0DQ[62]
104	3	29	AA10	VSS	105	D35	DDR0DQ[63]
105	3	30	AA9	VSS	106	J4	DDR0DQ[7]
106	3	31	AA8	VSS	107	F2	DDR0DQ[8]
107	3	32	AA7	VSS	108	F1	DDR0DQ[9]
108	3	33	AA6	VSS	109	G4	DDR0DQSN[0]
109	3	34	AA5	VSS	110	H2	DDR0DQSN[1]
110	3	35	AA4	DDR0CB[2]	111	G1	DDR0DQSN[10]
111	3	36	AA3	DDR0CB[6]	112	N4	DDR0DQSN[11]
112	3	37	AA2	VSS	113	P1	DDR0DQSN[12]
113	3	38	AA1	VSS	114	W37	DDR0DQSN[13]
114	4	1	Y38	VSS	115	R37	DDR0DQSN[14]
115	4	2	Y37	DDR0DQSP[13]	116	H37	DDR0DQSN[15]
116	4	3	Y36	DDR0DQ[33]	117	G35	DDR0DQSN[16]
117	4	4	Y35	DDR0DQ[36]	118	W2	DDR0DQSN[17]
118	4	5	Y34	VSS	119	P5	DDR0DQSN[2]
119	4	6	Y33	VSS	120	R2	DDR0DQSN[3]
120	4	7	Y32	DDR1ODT[3]	121	W36	DDR0DQSN[4]
121	4	8	Y31	VCCADDRIO_1P5	122	P38	DDR0DQSN[5]
122	4	9	Y30	DDR1ODT[2]	123	G38	DDR0DQSN[6]
123	4	10	Y29	DDR1CS_N[2]	124	F35	DDR0DQSN[7]
124	4	11	Y28	DDR1CS_N[3]	125	Y3	DDR0DQSN[8]
125	4	12	Y27	DDR1CS_N[1]	126	F4	DDR0DQSN[9]
126	4	13	Y26	VCCADDRIO_1P5	127	G5	DDR0DQSP[0]
127	4	14	Y25	DDR1CKP[3]	128	H1	DDR0DQSP[1]
128	4	15	Y24	DDR1CKN[3]	129	G2	DDR0DQSP[10]
129	4	16	Y23	DDR1MA[10]	130	N5	DDR0DQSP[11]
130	4	17	Y22	DDR1MA[0]	131	P2	DDR0DQSP[12]
131	4	18	Y21	VCCADDRIO_1P5	132	Y37	DDR0DQSP[13]
132	4	19	Y20	DDR1MA[2]	133	R38	DDR0DQSP[14]
133	4	20	Y19	DDR1MA[6]	134	H38	DDR0DQSP[15]
134	4	21	Y18	DDR0ERR_N	135	G34	DDR0DQSP[16]
135	4	22	Y17	DDR0ODT[5]	136	W3	DDR0DQSP[17]
136	4	23	Y16	VCCADDRIO_1P5	137	P4	DDR0DQSP[2]
137	4	24	Y15	DDR0CKE[5]	138	R1	DDR0DQSP[3]
138	4	25	Y14	DDR0CKE[4]	139	W35	DDR0DQSP[4]
139	4	26	Y13	DDR0CS_N[9]	140	P37	DDR0DQSP[5]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 5 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
140	4	27	Y12	VSS	141	G37	DDR0DQSP[6]
141	4	28	Y11	DDR1DQ[27]	142	F34	DDR0DQSP[7]
142	4	29	Y10	DDR1DQ[31]	143	Y2	DDR0DQSP[8]
143	4	30	Y9	VSS	144	E4	DDR0DQSP[9]
144	4	31	Y8	DDR1DQ[19]	145	Y18	DDR0ERR_N
145	4	32	Y7	DDR1DQ[23]	146	AB23	DDR0MA[0]
146	4	33	Y6	VSS	147	AA20	DDR0MA[1]
147	4	34	Y5	VSS	148	AB24	DDR0MA[10]
148	4	35	Y4	DDR0CB[3]	149	AB17	DDR0MA[11]
149	4	36	Y3	DDR0DQSN[8]	150	AA15	DDR0MA[12]
150	4	37	Y2	DDR0DQSP[8]	151	AA21	DDR0MA[13]
151	4	38	Y1	VSS	152	AB15	DDR0MA[14]
152	5	1	W38	VSS	153	AC15	DDR0MA[15]
153	5	2	W37	DDR0DQSN[13]	154	AC22	DDR0MA[2]
154	5	3	W36	DDR0DQSN[4]	155	AC20	DDR0MA[3]
155	5	4	W35	DDR0DQSP[4]	156	AB20	DDR0MA[4]
156	5	5	W34	DDR0DQ[34]	157	AA18	DDR0MA[5]
157	5	6	W33	VSS	158	AB19	DDR0MA[6]
158	5	7	W32	DDR1CS_N[5]	159	AC18	DDR0MA[7]
159	5	8	W31	DDR1CS_N[6]	160	AB18	DDR0MA[8]
160	5	9	W30	DDR1CS_N[7]	161	AC17	DDR0MA[9]
161	5	10	W29	VCCADDRIO_1P5	162	AA30	DDR0ODT[0]
162	5	11	W28	DDR1ODT[1]	163	AC30	DDR0ODT[1]
163	5	12	W27	DDR1CS_N[0]	164	AC32	DDR0ODT[2]
164	5	13	W26	DDR1RAS_N	165	AC33	DDR0ODT[3]
165	5	14	W25	DDR1BA[0]	166	W15	DDR0ODT[4]
166	5	15	W24	VCCADDRIO_1P5	167	Y17	DDR0ODT[5]
167	5	16	W23	DDR1CKP[2]	168	AC23	DDR0PAR
168	5	17	W22	DDR1CKN[2]	169	AA23	DDR0RAS_N
169	5	18	W21	DDR1CKN[1]	170	AA12	DDR0RESET_N
170	5	19	W20	DDR1CKP[1]	171	T20	DDR0TXVREF
171	5	20	W19	VCCADDRIO_1P5	172	AA25	NC
172	5	21	W18	DDR1C0	173	AA26	NC
173	5	22	W17	DDR1MA[7]	174	AA22	DDR0WE_N
174	5	23	W16	DDR1MA[11]	175	V17	DDR1ACT_N
175	5	24	W15	DDR0ODT[4]	176	W25	DDR1BA[0]
176	5	25	W14	VCCADDRIO_1P5	177	V24	DDR1BA[1]
177	5	26	W13	DDR0CS_N[8]	178	U13	DDR1BA[2]
178	5	27	W12	VSS	179	W18	DDR1C0
179	5	28	W11	DDR1DQ[26]	180	V27	DDR1CAS_N
180	5	29	W10	DDR1DQ[30]	181	AB7	DDR1CB[0]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 6 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
181	5	30	W9	VSS	182	AC7	DDR1CB[1]
182	5	31	W8	DDR1DQ[18]	183	AB11	DDR1CB[2]
183	5	32	W7	DDR1DQ[22]	184	AC11	DDR1CB[3]
184	5	33	W6	VSS	185	AB6	DDR1CB[4]
185	5	34	W5	DDR0CB[5]	186	AC6	DDR1CB[5]
186	5	35	W4	DDR0CB[1]	187	AB10	DDR1CB[6]
187	5	36	W3	DDR0DQSP[17]	188	AC10	DDR1CB[7]
188	5	37	W2	DDR0DQSN[17]	189	V12	DDR1CKE[0]
189	5	38	W1	VSS	190	T13	DDR1CKE[1]
190	6	1	V38	VSS	191	T15	DDR1CKE[2]
191	6	2	V37	VSS	192	V13	DDR1CKE[3]
192	6	3	V36	DDR0DQ[38]	193	T18	DDR1CKE[4]
193	6	4	V35	DDR0DQ[39]	194	N14	DDR1CKE[5]
194	6	5	V34	DDR0DQ[35]	195	V23	DDR1CKN[0]
195	6	6	V33	VSS	196	W21	DDR1CKN[1]
196	6	7	V32	VSS	197	W22	DDR1CKN[2]
197	6	8	V31	VSS	198	Y24	DDR1CKN[3]
198	6	9	V30	VSS	199	V22	DDR1CKP[0]
199	6	10	V29	DDR1CS_N[4]	200	W20	DDR1CKP[1]
200	6	11	V28	DDR1ODT[0]	201	W23	DDR1CKP[2]
201	6	12	V27	DDR1CAS_N	202	Y25	DDR1CKP[3]
202	6	13	V26	VCCADDRIO_1P5	203	W27	DDR1CS_N[0]
203	6	14	V25	DDR1WE_N	204	Y27	DDR1CS_N[1]
204	6	15	V24	DDR1BA[1]	205	Y29	DDR1CS_N[2]
205	6	16	V23	DDR1CKN[0]	206	Y28	DDR1CS_N[3]
206	6	17	V22	DDR1CKP[0]	207	V29	DDR1CS_N[4]
207	6	18	V21	VCCADDRIO_1P5	208	W32	DDR1CS_N[5]
208	6	19	V20	DDR1PAR	209	W31	DDR1CS_N[6]
209	6	20	V19	DDR1MA[3]	210	W30	DDR1CS_N[7]
210	6	21	V18	DDR1MA[4]	211	P13	DDR1CS_N[8]
211	6	22	V17	DDR1ACT_N	212	R14	DDR1CS_N[9]
212	6	23	V16	VCCADDRIO_1P5	213	J10	DDR1DQ[0]
213	6	24	V15	DDR1MA[8]	214	J11	DDR1DQ[1]
214	6	25	V14	DDR1MA[12]	215	N7	DDR1DQ[10]
215	6	26	V13	DDR1CKE[3]	216	N8	DDR1DQ[11]
216	6	27	V12	DDR1CKE[0]	217	H8	DDR1DQ[12]
217	6	28	V11	DDR1DQSP[3]	218	J8	DDR1DQ[13]
218	6	29	V10	DDR1DQSN[3]	219	M7	DDR1DQ[14]
219	6	30	V9	VSS	220	M8	DDR1DQ[15]
220	6	31	V8	DDR1DQSP[2]	221	R7	DDR1DQ[16]
221	6	32	V7	DDR1DQSN[2]	222	T7	DDR1DQ[17]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 7 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
222	6	33	V6	VSS	223	W8	DDR1DQ[18]
223	6	34	V5	DDR0CB[4]	224	Y8	DDR1DQ[19]
224	6	35	V4	DDR0CB[0]	225	M11	DDR1DQ[2]
225	6	36	V3	VSS	226	R8	DDR1DQ[20]
226	6	37	V2	VSS	227	T8	DDR1DQ[21]
227	6	38	V1	VSS	228	W7	DDR1DQ[22]
228	7	1	U38	DDR0DQ[44]	229	Y7	DDR1DQ[23]
229	7	2	U37	DDR0DQ[45]	230	R10	DDR1DQ[24]
230	7	3	U36	VSS	231	T10	DDR1DQ[25]
231	7	4	U35	VSS	232	W11	DDR1DQ[26]
232	7	5	U34	VSS	233	Y11	DDR1DQ[27]
233	7	6	U33	VSS	234	R11	DDR1DQ[28]
234	7	7	U32	DDR1DQ[32]	235	T11	DDR1DQ[29]
235	7	8	U31	DDR1DQ[36]	236	N11	DDR1DQ[3]
236	7	9	U30	VSS	237	W10	DDR1DQ[30]
237	7	10	U29	NC	238	Y10	DDR1DQ[31]
238	7	11	U28	NC	239	U32	DDR1DQ[32]
239	7	12	U27	DDR1MA[13]	240	T32	DDR1DQ[33]
240	7	13	U26	VSS	241	M31	DDR1DQ[34]
241	7	14	U25	TRIG[1]	242	M32	DDR1DQ[35]
242	7	15	U24	VCCADDRIO_1P5	243	U31	DDR1DQ[36]
243	7	16	U23	SA0	244	T31	DDR1DQ[37]
244	7	17	U22	SCL	245	N32	DDR1DQ[38]
245	7	18	U21	TRST_N	246	N31	DDR1DQ[39]
246	7	19	U20	NC	247	H11	DDR1DQ[4]
247	7	20	U19	VCCADDRIO_1P5	248	T35	DDR1DQ[40]
248	7	21	U18	DDR1MA[5]	249	R35	DDR1DQ[41]
249	7	22	U17	DDR1MA[1]	250	M34	DDR1DQ[42]
250	7	23	U16	DDR1MA[9]	251	L34	DDR1DQ[43]
251	7	24	U15	VCCADDRIO_1P5	252	T34	DDR1DQ[44]
252	7	25	U14	DDR1ERR_N	253	R34	DDR1DQ[45]
253	7	26	U13	DDR1BA[2]	254	M35	DDR1DQ[46]
254	7	27	U12	VSS	255	L35	DDR1DQ[47]
255	7	28	U11	DDR1DQSP[12]	256	M29	DDR1DQ[48]
256	7	29	U10	DDR1DQSN[12]	257	L29	DDR1DQ[49]
257	7	30	U9	VSS	258	H10	DDR1DQ[5]
258	7	31	U8	DDR1DQSP[11]	259	G28	DDR1DQ[50]
259	7	32	U7	DDR1DQSN[11]	260	H28	DDR1DQ[51]
260	7	33	U6	VSS	261	L28	DDR1DQ[52]
261	7	34	U5	VSS	262	M28	DDR1DQ[53]
262	7	35	U4	VSS	263	H29	DDR1DQ[54]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 8 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
263	7	36	U3	VSS	264	G29	DDR1DQ[55]
264	7	37	U2	DDR0DQ[26]	265	K32	DDR1DQ[56]
265	7	38	U1	DDR0DQ[27]	266	J32	DDR1DQ[57]
266	8	1	T38	DDR0DQ[40]	267	F31	DDR1DQ[58]
267	8	2	T37	DDR0DQ[41]	268	E31	DDR1DQ[59]
268	8	3	T36	VSS	269	M10	DDR1DQ[6]
269	8	4	T35	DDR1DQ[40]	270	K31	DDR1DQ[60]
270	8	5	T34	DDR1DQ[44]	271	J31	DDR1DQ[61]
271	8	6	T33	VSS	272	F32	DDR1DQ[62]
272	8	7	T32	DDR1DQ[33]	273	E32	DDR1DQ[63]
273	8	8	T31	DDR1DQ[37]	274	N10	DDR1DQ[7]
274	8	9	T30	VSS	275	H7	DDR1DQ[8]
275	8	10	T29	TRIG[2]	276	J7	DDR1DQ[9]
276	8	11	T28	VCCADDRIO_1P5	277	L10	DDR1DQSN[0]
277	8	12	T27	NC	278	L7	DDR1DQSN[1]
278	8	13	T26	VSS	279	K7	DDR1DQSN[10]
279	8	14	T25	BIREF_NPAD	280	U7	DDR1DQSN[11]
280	8	15	T24	NC	281	U10	DDR1DQSN[12]
281	8	16	T23	VSS	282	R31	DDR1DQSN[13]
282	8	17	T22	VSS	283	P35	DDR1DQSN[14]
283	8	18	T21	DDR1TXVREF	284	K29	DDR1DQSN[15]
284	8	19	T20	DDR0TXVREF	285	H32	DDR1DQSN[16]
285	8	20	T19	DDR_COMP	286	AC8	DDR1DQSN[17]
286	8	21	T18	DDR1CKE[4]	287	V7	DDR1DQSN[2]
287	8	22	T17	DDR1ODT[5]	288	V10	DDR1DQSN[3]
288	8	23	T16	DDR1MA[14]	289	P32	DDR1DQSN[4]
289	8	24	T15	DDR1CKE[2]	290	N35	DDR1DQSN[5]
290	8	25	T14	VCCADDRIO_1P5	291	J28	DDR1DQSN[6]
291	8	26	T13	DDR1CKE[1]	292	G32	DDR1DQSN[7]
292	8	27	T12	VSS	293	AB9	DDR1DQSN[8]
293	8	28	T11	DDR1DQ[29]	294	K11	DDR1DQSN[9]
294	8	29	T10	DDR1DQ[25]	295	L11	DDR1DQSP[0]
295	8	30	T9	VSS	296	L8	DDR1DQSP[1]
296	8	31	T8	DDR1DQ[21]	297	K8	DDR1DQSP[10]
297	8	32	T7	DDR1DQ[17]	298	U8	DDR1DQSP[11]
298	8	33	T6	VSS	299	U11	DDR1DQSP[12]
299	8	34	T5	DDR0DQ[19]	300	R32	DDR1DQSP[13]
300	8	35	T4	DDR0DQ[18]	301	P34	DDR1DQSP[14]
301	8	36	T3	VSS	302	K28	DDR1DQSP[15]
302	8	37	T2	DDR0DQ[30]	303	H31	DDR1DQSP[16]
303	8	38	T1	DDR0DQ[31]	304	AB8	DDR1DQSP[17]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 9 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
304	9	1	R38	DDR0DQSP[14]	305	V8	DDR1DQSP[2]
305	9	2	R37	DDR0DQSN[14]	306	V11	DDR1DQSP[3]
306	9	3	R36	VSS	307	P31	DDR1DQSP[4]
307	9	4	R35	DDR1DQ[41]	308	N34	DDR1DQSP[5]
308	9	5	R34	DDR1DQ[45]	309	J29	DDR1DQSP[6]
309	9	6	R33	VSS	310	G31	DDR1DQSP[7]
310	9	7	R32	DDR1DQSP[13]	311	AC9	DDR1DQSP[8]
311	9	8	R31	DDR1DQSN[13]	312	K10	DDR1DQSP[9]
312	9	9	R30	VSS	313	U14	DDR1ERR_N
313	9	10	R29	TDO	314	Y22	DDR1MA[0]
314	9	11	R28	RST_N	315	U17	DDR1MA[1]
315	9	12	R27	NC	316	Y23	DDR1MA[10]
316	9	13	R26	VSS	317	W16	DDR1MA[11]
317	9	14	R25	TRIG[0]	318	V14	DDR1MA[12]
318	9	15	R24	VSS	319	U27	DDR1MA[13]
319	9	16	R23	VSS	320	T16	DDR1MA[14]
320	9	17	R22	VSS	321	R13	DDR1MA[15]
321	9	18	R21	VSS	322	Y20	DDR1MA[2]
322	9	19	R20	VSS	323	V19	DDR1MA[3]
323	9	20	R19	VSS	324	V18	DDR1MA[4]
324	9	21	R18	VSS	325	U18	DDR1MA[5]
325	9	22	R17	VSS	326	Y19	DDR1MA[6]
326	9	23	R16	VSS	327	W17	DDR1MA[7]
327	9	24	R15	DDR1RESET_N	328	V15	DDR1MA[8]
328	9	25	R14	DDR1CS_N[9]	329	U16	DDR1MA[9]
329	9	26	R13	DDR1MA[15]	330	V28	DDR1ODT[0]
330	9	27	R12	VSS	331	W28	DDR1ODT[1]
331	9	28	R11	DDR1DQ[28]	332	Y30	DDR1ODT[2]
332	9	29	R10	DDR1DQ[24]	333	Y32	DDR1ODT[3]
333	9	30	R9	VSS	334	P14	DDR1ODT[4]
334	9	31	R8	DDR1DQ[20]	335	T17	DDR1ODT[5]
335	9	32	R7	DDR1DQ[16]	336	V20	DDR1PAR
336	9	33	R6	VSS	337	W26	DDR1RAS_N
337	9	34	R5	DDR0DQ[23]	338	R15	DDR1RESET_N
338	9	35	R4	DDR0DQ[22]	339	T21	DDR1TXVREF
339	9	36	R3	VSS	340	U28	NC
340	9	37	R2	DDR0DQSN[3]	341	U29	NC
341	9	38	R1	DDR0DQSP[3]	342	V25	DDR1WE_N
342	10	1	P38	DDR0DQSN[5]	343	U26	VSS
343	10	2	P37	DDR0DQSP[5]	344	R26	VSS
344	10	3	P36	VSS	345	K14	NC

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 10 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
345	10	4	P35	DDR1DQSN[14]	346	L14	NC
346	10	5	P34	DDR1DQSP[14]	347	M13	REFCK100N
347	10	6	P33	VSS	348	L13	REFCK100P
348	10	7	P32	DDR1DQSN[4]	349	R28	RST_N
349	10	8	P31	DDR1DQSP[4]	350	L25	RSVD
350	10	9	P30	VSS	351	U23	SA0
351	10	10	P29	NC	352	U22	SCL
352	10	11	P28	NC	353	N26	SDA
353	10	12	P27	NC	354	T22	VSS
354	10	13	P26	VSS	355	T27	NC
355	10	14	P25	NC	356	P28	NC
356	10	15	P24	VCCADDRDLL_1P5	357	M14	TCK
357	10	16	P23	VSS	358	N13	TDI
358	10	17	P22	VCCDCORE_1P0	359	R29	TDO
359	10	18	P21	VCCDCORE_1P0	360	N25	TMS
360	10	19	P20	VCCDCORE_1P0	361	R25	TRIG[0]
361	10	20	P19	VCCDCORE_1P0	362	U25	TRIG[1]
362	10	21	P18	VCCDCORE_1P0	363	T29	TRIG[2]
363	10	22	P17	VCCDCORE_1P0	364	U21	TRST_N
364	10	23	P16	VSS	365	P24	VCCADDRDLL_1P5
365	10	24	P15	VCCADDRDLL_1P5	366	P15	VCCADDRDLL_1P5
366	10	25	P14	DDR1ODT[4]	367	N24	VCCADDRDLL_1P5
367	10	26	P13	DDR1CS_N[8]	368	N15	VCCADDRDLL_1P5
368	10	27	P12	VSS	369	AC24	VCCADDRIO_1P5
369	10	28	P11	VSS	370	AC19	VCCADDRIO_1P5
370	10	29	P10	VSS	371	AC14	VCCADDRIO_1P5
371	10	30	P9	VSS	372	AB31	VCCADDRIO_1P5
372	10	31	P8	VSS	373	AB29	VCCADDRIO_1P5
373	10	32	P7	VSS	374	AB26	VCCADDRIO_1P5
374	10	33	P6	VSS	375	AB21	VCCADDRIO_1P5
375	10	34	P5	DDR0DQSN[2]	376	AB16	VCCADDRIO_1P5
376	10	35	P4	DDR0DQSP[2]	377	AA29	VCCADDRIO_1P5
377	10	36	P3	VSS	378	AA24	VCCADDRIO_1P5
378	10	37	P2	DDR0DQSP[12]	379	AA19	VCCADDRIO_1P5
379	10	38	P1	DDR0DQSN[12]	380	AA14	VCCADDRIO_1P5
380	11	1	N38	DDR0DQ[46]	381	Y31	VCCADDRIO_1P5
381	11	2	N37	DDR0DQ[47]	382	Y26	VCCADDRIO_1P5
382	11	3	N36	VSS	383	Y21	VCCADDRIO_1P5
383	11	4	N35	DDR1DQSN[5]	384	Y16	VCCADDRIO_1P5
384	11	5	N34	DDR1DQSP[5]	385	W29	VCCADDRIO_1P5
385	11	6	N33	VSS	386	W24	VCCADDRIO_1P5

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 11 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
386	11	7	N32	DDR1DQ[38]	387	W19	VCCADDRIO_1P5
387	11	8	N31	DDR1DQ[39]	388	W14	VCCADDRIO_1P5
388	11	9	N30	VSS	389	V26	VCCADDRIO_1P5
389	11	10	N29	VSS	390	V21	VCCADDRIO_1P5
390	11	11	N28	VSS	391	V16	VCCADDRIO_1P5
391	11	12	N27	VSS	392	U24	VCCADDRIO_1P5
392	11	13	N26	SDA	393	U19	VCCADDRIO_1P5
393	11	14	N25	TMS	394	U15	VCCADDRIO_1P5
394	11	15	N24	VCCADDRDLL_1P5	395	T28	VCCADDRIO_1P5
395	11	16	N23	VSS	396	T14	VCCADDRIO_1P5
396	11	17	N22	VCCDCORE_1P0	397	M26	VCCDCORE_1P0
397	11	18	N21	VCCDCORE_1P0	398	L15	VCCAIO_PWRGOOD
398	11	19	N20	VCCDCORE_1P0	399	L26	VCCAMISCTS_1P5
399	11	20	N19	VCCDCORE_1P0	400	L22	VCCAVMSEIO_1P35
400	11	21	N18	VCCDCORE_1P0	401	L21	VCCAVMSEIO_1P35
401	11	22	N17	VCCDCORE_1P0	402	L18	VCCAVMSEIO_1P35
402	11	23	N16	VSS	403	L17	VCCAVMSEIO_1P35
403	11	24	N15	VCCADDRDLL_1P5	404	K22	VCCAVMSEIO_1P35
404	11	25	N14	DDR1CKE[5]	405	K21	VCCAVMSEIO_1P35
405	11	26	N13	TDI	406	K18	VCCAVMSEIO_1P35
406	11	27	N12	VSS	407	K17	VCCAVMSEIO_1P35
407	11	28	N11	DDR1DQ[3]	408	K15	VCCAVMSEPLL_1P5
408	11	29	N10	DDR1DQ[7]	409	J15	VCCAVMSEPLL_1P5
409	11	30	N9	VSS	410	M15	VCCD_PWRGOOD
410	11	31	N8	DDR1DQ[11]	411	P22	VCCDCORE_1P0
411	11	32	N7	DDR1DQ[10]	412	P21	VCCDCORE_1P0
412	11	33	N6	VSS	413	P20	VCCDCORE_1P0
413	11	34	N5	DDR0DQSP[11]	414	P19	VCCDCORE_1P0
414	11	35	N4	DDR0DQSN[11]	415	P18	VCCDCORE_1P0
415	11	36	N3	VSS	416	P17	VCCDCORE_1P0
416	11	37	N2	DDR0DQ[24]	417	N22	VCCDCORE_1P0
417	11	38	N1	DDR0DQ[25]	418	N21	VCCDCORE_1P0
418	12	1	M38	DDR0DQ[42]	419	N20	VCCDCORE_1P0
419	12	2	M37	DDR0DQ[43]	420	N19	VCCDCORE_1P0
420	12	3	M36	VSS	421	N18	VCCDCORE_1P0
421	12	4	M35	DDR1DQ[46]	422	N17	VCCDCORE_1P0
422	12	5	M34	DDR1DQ[42]	423	M22	VCCDCORE_1P0
423	12	6	M33	VSS	424	M17	VCCDCORE_1P0
424	12	7	M32	DDR1DQ[35]	425	L20	VCCDVMSEIO_1P0
425	12	8	M31	DDR1DQ[34]	426	L19	VCCDVMSEIO_1P0
426	12	9	M30	VSS	427	K20	VCCDVMSEIO_1P0

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 12 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
427	12	10	M29	DDR1DQ[48]	428	K19	VCCDVMSEIO_1P0
428	12	11	M28	DDR1DQ[53]	429	P27	NC
429	12	12	M27	VSS	430	P29	NC
430	12	13	M26	VCCDCORE_1P0	431	K24	NC
431	12	14	M25	VSS	432	K13	NC
432	12	15	M24	VSS	433	G12	VMSE_CRES_N
433	12	16	M23	VSS	434	G13	VMSE_CRES_P
434	12	17	M22	VCCDCORE_1P0	435	L24	VMSE_ERR_N
435	12	18	M21	VSS	436	G11	NC
436	12	19	M20	VSS	437	H13	NC
437	12	20	M19	VSS	438	J13	NC
438	12	21	M18	VSS	439	G10	NC
439	12	22	M17	VCCDCORE_1P0	440	J25	NC
440	12	23	M16	VSS	441	J24	VMSE_REXT
441	12	24	M15	VCCD_PWRGOOD	442	K26	NC
442	12	25	M14	TCK	443	H20	VMSECKN
443	12	26	M13	REFCK100N	444	G20	VMSECKP
444	12	27	M12	VSS	445	H15	VMSECMD_N[0]
445	12	28	M11	DDR1DQ[2]	446	G19	VMSECMD_N[1]
446	12	29	M10	DDR1DQ[6]	447	H25	VMSECMD_N[10]
447	12	30	M9	VSS	448	G25	VMSECMD_N[11]
448	12	31	M8	DDR1DQ[15]	449	H26	VMSECMD_N[12]
449	12	32	M7	DDR1DQ[14]	450	G22	VMSECMD_N[13]
450	12	33	M6	VSS	451	G26	VMSECMD_N[14]
451	12	34	M5	DDR0DQ[16]	452	G23	VMSECMD_N[15]
452	12	35	M4	DDR0DQ[17]	453	H23	VMSECMD_N[16]
453	12	36	M3	VSS	454	G15	VMSECMD_N[2]
454	12	37	M2	DDR0DQ[28]	455	H16	VMSECMD_N[3]
455	12	38	M1	DDR0DQ[29]	456	H18	VMSECMD_N[4]
456	13	1	L38	VSS	457	H19	VMSECMD_N[5]
457	13	2	L37	VSS	458	G18	VMSECMD_N[6]
458	13	3	L36	VSS	459	G16	VMSECMD_N[7]
459	13	4	L35	DDR1DQ[47]	460	H14	VMSECMD_N[8]
460	13	5	L34	DDR1DQ[43]	461	H22	VMSECMD_N[9]
461	13	6	L33	VSS	462	B6	VMSEDQ[0]
462	13	7	L32	VSS	463	A7	VMSEDQ[1]
463	13	8	L31	VSS	464	D10	VMSEDQ[10]
464	13	9	L30	VSS	465	E10	VMSEDQ[11]
465	13	10	L29	DDR1DQ[49]	466	D6	VMSEDQ[12]
466	13	11	L28	DDR1DQ[52]	467	E7	VMSEDQ[13]
467	13	12	L27	VSS	468	E9	VMSEDQ[14]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 13 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
468	13	13	L26	VCCAMISCTS_1P5	469	D9	VMSEDQ[15]
469	13	14	L25	RSVD	470	B12	VMSEDQ[16]
470	13	15	L24	VMSE_ERR_N	471	A13	VMSEDQ[17]
471	13	16	L23	VSS	472	B15	VMSEDQ[18]
472	13	17	L22	VCCAVMSEIO_1P35	473	B16	VMSEDQ[19]
473	13	18	L21	VCCAVMSEIO_1P35	474	B9	VMSEDQ[2]
474	13	19	L20	VCCDVMSEIO_1P0	475	B13	VMSEDQ[20]
475	13	20	L19	VCCDVMSEIO_1P0	476	A12	VMSEDQ[21]
476	13	21	L18	VCCAVMSEIO_1P35	477	A16	VMSEDQ[22]
477	13	22	L17	VCCAVMSEIO_1P35	478	A15	VMSEDQ[23]
478	13	23	L16	VSS	479	E12	VMSEDQ[24]
479	13	24	L15	VCCAIO_PWRGOOD	480	D13	VMSEDQ[25]
480	13	25	L14	NC	481	D16	VMSEDQ[26]
481	13	26	L13	REFCK100P	482	E16	VMSEDQ[27]
482	13	27	L12	VSS	483	D12	VMSEDQ[28]
483	13	28	L11	DDR1DQSP[0]	484	E13	VMSEDQ[29]
484	13	29	L10	DDR1DQSN[0]	485	B10	VMSEDQ[3]
485	13	30	L9	VSS	486	E15	VMSEDQ[30]
486	13	31	L8	DDR1DQSP[1]	487	D15	VMSEDQ[31]
487	13	32	L7	DDR1DQSN[1]	488	E18	VMSEDQ[32]
488	13	33	L6	VSS	489	D19	VMSEDQ[33]
489	13	34	L5	DDR0DQ[20]	490	D22	VMSEDQ[34]
490	13	35	L4	DDR0DQ[21]	491	E22	VMSEDQ[35]
491	13	36	L3	VSS	492	D18	VMSEDQ[36]
492	13	37	L2	VSS	493	E19	VMSEDQ[37]
493	13	38	L1	VSS	494	E21	VMSEDQ[38]
494	14	1	K38	DDR0DQ[52]	495	D21	VMSEDQ[39]
495	14	2	K37	DDR0DQ[53]	496	B7	VMSEDQ[4]
496	14	3	K36	VSS	497	B24	VMSEDQ[40]
497	14	4	K35	VSS	498	A25	VMSEDQ[41]
498	14	5	K34	VSS	499	B27	VMSEDQ[42]
499	14	6	K33	VSS	500	B28	VMSEDQ[43]
500	14	7	K32	DDR1DQ[56]	501	B25	VMSEDQ[44]
501	14	8	K31	DDR1DQ[60]	502	A24	VMSEDQ[45]
502	14	9	K30	VSS	503	A28	VMSEDQ[46]
503	14	10	K29	DDR1DQSN[15]	504	A27	VMSEDQ[47]
504	14	11	K28	DDR1DQSP[15]	505	E24	VMSEDQ[48]
505	14	12	K27	VSS	506	D25	VMSEDQ[49]
506	14	13	K26	NC	507	A6	VMSEDQ[5]
507	14	14	K25	VSS	508	D29	VMSEDQ[50]
508	14	15	K24	NC	509	E29	VMSEDQ[51]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 14 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
509	14	16	K23	VSS	510	D24	VMSEDQ[52]
510	14	17	K22	VCCAVMSEIO_1P35	511	E25	VMSEDQ[53]
511	14	18	K21	VCCAVMSEIO_1P35	512	E28	VMSEDQ[54]
512	14	19	K20	VCCDVMSEIO_1P0	513	D28	VMSEDQ[55]
513	14	20	K19	VCCDVMSEIO_1P0	514	B30	VMSEDQ[56]
514	14	21	K18	VCCAVMSEIO_1P35	515	A31	VMSEDQ[57]
515	14	22	K17	VCCAVMSEIO_1P35	516	B33	VMSEDQ[58]
516	14	23	K16	VSS	517	B35	VMSEDQ[59]
517	14	24	K15	VCCAVMSEPLL_1P5	518	A10	VMSEDQ[6]
518	14	25	K14	NC	519	B31	VMSEDQ[60]
519	14	26	K13	NC	520	A30	VMSEDQ[61]
520	14	27	K12	VSS	521	B34	VMSEDQ[62]
521	14	28	K11	DDR1DQSN[9]	522	A33	VMSEDQ[63]
522	14	29	K10	DDR1DQSP[9]	523	A9	VMSEDQ[7]
523	14	30	K9	VSS	524	E6	VMSEDQ[8]
524	14	31	K8	DDR1DQSP[10]	525	D7	VMSEDQ[9]
525	14	32	K7	DDR1DQSN[10]	526	C8	VMSEDQSN[0]
526	14	33	K6	VSS	527	E8	VMSEDQSN[1]
527	14	34	K5	VSS	528	B14	VMSEDQSN[2]
528	14	35	K4	VSS	529	E14	VMSEDQSN[3]
529	14	36	K3	VSS	530	E20	VMSEDQSN[4]
530	14	37	K2	DDR0DQ[10]	531	B26	VMSEDQSN[5]
531	14	38	K1	DDR0DQ[11]	532	E27	VMSEDQSN[6]
532	15	1	J38	DDR0DQ[48]	533	B32	VMSEDQSN[7]
533	15	2	J37	DDR0DQ[49]	534	C20	VMSEDQSN[8]
534	15	3	J36	VSS	535	B8	VMSEDQSP[0]
535	15	4	J35	DDR0DQ[56]	536	F8	VMSEDQSP[1]
536	15	5	J34	DDR0DQ[60]	537	C14	VMSEDQSP[2]
537	15	6	J33	VSS	538	F14	VMSEDQSP[3]
538	15	7	J32	DDR1DQ[57]	539	F20	VMSEDQSP[4]
539	15	8	J31	DDR1DQ[61]	540	C26	VMSEDQSP[5]
540	15	9	J30	VSS	541	D27	VMSEDQSP[6]
541	15	10	J29	DDR1DQSP[6]	542	C32	VMSEDQSP[7]
542	15	11	J28	DDR1DQSN[6]	543	B20	VMSEDQSP[8]
543	15	12	J27	VSS	544	B18	VMSEECC[0]
544	15	13	J26	VSS	545	A19	VMSEECC[1]
545	15	14	J25	NC	546	B21	VMSEECC[2]
546	15	15	J24	VMSE_REXT	547	B22	VMSEECC[3]
547	15	16	J23	VSS	548	B19	VMSEECC[4]
548	15	17	J22	VSS	549	A18	VMSEECC[5]
549	15	18	J21	VSS	550	A22	VMSEECC[6]

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 15 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
550	15	19	J20	VSS	551	A21	VMSEECC[7]
551	15	20	J19	VSS	552	AC37	VSS
552	15	21	J18	VSS	553	AC36	VSS
553	15	22	J17	VSS	554	AC35	VSS
554	15	23	J16	VSS	555	AC34	VSS
555	15	24	J15	VCCAVMSEPLL_1P5	556	AC12	VSS
556	15	25	J14	VSS	557	AC5	VSS
557	15	26	J13	NC	558	AC4	VSS
558	15	27	J12	VSS	559	AC3	VSS
559	15	28	J11	DDR1DQ[1]	560	AC2	VSS
560	15	29	J10	DDR1DQ[0]	561	AB38	VSS
561	15	30	J9	VSS	562	AB37	VSS
562	15	31	J8	DDR1DQ[13]	563	AB36	VSS
563	15	32	J7	DDR1DQ[9]	564	AB35	VSS
564	15	33	J6	VSS	565	AB34	VSS
565	15	34	J5	DDR0DQ[3]	566	AB12	VSS
566	15	35	J4	DDR0DQ[7]	567	AB5	VSS
567	15	36	J3	VSS	568	AB3	VSS
568	15	37	J2	DDR0DQ[14]	569	AB2	VSS
569	15	38	J1	DDR0DQ[15]	570	AB1	VSS
570	16	1	H38	DDR0DQSP[15]	571	AA38	VSS
571	16	2	H37	DDR0DQSN[15]	572	AA37	VSS
572	16	3	H36	VSS	573	AA34	VSS
573	16	4	H35	DDR0DQ[57]	574	AA11	VSS
574	16	5	H34	DDR0DQ[61]	575	AA10	VSS
575	16	6	H33	VSS	576	AA9	VSS
576	16	7	H32	DDR1DQSN[16]	577	AA8	VSS
577	16	8	H31	DDR1DQSP[16]	578	AA7	VSS
578	16	9	H30	VSS	579	AA6	VSS
579	16	10	H29	DDR1DQ[54]	580	AA5	VSS
580	16	11	H28	DDR1DQ[51]	581	AA2	VSS
581	16	12	H27	VSS	582	AA1	VSS
582	16	13	H26	VMSECMD_N[12]	583	Y38	VSS
583	16	14	H25	VMSECMD_N[10]	584	Y34	VSS
584	16	15	H24	VSS	585	Y33	VSS
585	16	16	H23	VMSECMD_N[16]	586	Y12	VSS
586	16	17	H22	VMSECMD_N[9]	587	Y9	VSS
587	16	18	H21	VSS	588	Y6	VSS
588	16	19	H20	VMSECKN	589	Y5	VSS
589	16	20	H19	VMSECMD_N[5]	590	Y1	VSS
590	16	21	H18	VMSECMD_N[4]	591	W38	VSS

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 16 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
591	16	22	H17	VSS	592	W33	VSS
592	16	23	H16	VMSECMD_N[3]	593	W12	VSS
593	16	24	H15	VMSECMD_N[0]	594	W9	VSS
594	16	25	H14	VMSECMD_N[8]	595	W6	VSS
595	16	26	H13	NC	596	W1	VSS
596	16	27	H12	VSS	597	V38	VSS
597	16	28	H11	DDR1DQ[4]	598	V37	VSS
598	16	29	H10	DDR1DQ[5]	599	V33	VSS
599	16	30	H9	VSS	600	V32	VSS
600	16	31	H8	DDR1DQ[12]	601	V31	VSS
601	16	32	H7	DDR1DQ[8]	602	V30	VSS
602	16	33	H6	VSS	603	V9	VSS
603	16	34	H5	DDR0DQ[2]	604	V6	VSS
604	16	35	H4	DDR0DQ[6]	605	V3	VSS
605	16	36	H3	VSS	606	V2	VSS
606	16	37	H2	DDR0DQSN[1]	607	V1	VSS
607	16	38	H1	DDR0DQSP[1]	608	U36	VSS
608	17	1	G38	DDR0DQSN[6]	609	U35	VSS
609	17	2	G37	DDR0DQSP[6]	610	U34	VSS
610	17	3	G36	VSS	611	U33	VSS
611	17	4	G35	DDR0DQSN[16]	612	U30	VSS
612	17	5	G34	DDR0DQSP[16]	613	U12	VSS
613	17	6	G33	VSS	614	U9	VSS
614	17	7	G32	DDR1DQSN[7]	615	U6	VSS
615	17	8	G31	DDR1DQSP[7]	616	U5	VSS
616	17	9	G30	VSS	617	U4	VSS
617	17	10	G29	DDR1DQ[55]	618	U3	VSS
618	17	11	G28	DDR1DQ[50]	619	T36	VSS
619	17	12	G27	VSS	620	T33	VSS
620	17	13	G26	VMSECMD_N[14]	621	T30	VSS
621	17	14	G25	VMSECMD_N[11]	622	T26	VSS
622	17	15	G24	VSS	623	T23	VSS
623	17	16	G23	VMSECMD_N[15]	624	T12	VSS
624	17	17	G22	VMSECMD_N[13]	625	T9	VSS
625	17	18	G21	VSS	626	T6	VSS
626	17	19	G20	VMSECKP	627	T3	VSS
627	17	20	G19	VMSECMD_N[1]	628	R36	VSS
628	17	21	G18	VMSECMD_N[6]	629	R33	VSS
629	17	22	G17	VSS	630	R30	VSS
630	17	23	G16	VMSECMD_N[7]	631	R24	VSS
631	17	24	G15	VMSECMD_N[2]	632	R23	VSS

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 17 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
632	17	25	G14	VSS	633	R22	VSS
633	17	26	G13	VMSE_CRES_P	634	R21	VSS
634	17	27	G12	VMSE_CRES_N	635	R20	VSS
635	17	28	G11	NC	636	R19	VSS
636	17	29	G10	NC	637	R18	VSS
637	17	30	G9	VSS	638	R17	VSS
638	17	31	G8	VSS	639	R16	VSS
639	17	32	G7	VSS	640	R12	VSS
640	17	33	G6	VSS	641	R9	VSS
641	17	34	G5	DDR0DQSP[0]	642	R6	VSS
642	17	35	G4	DDR0DQSN[0]	643	R3	VSS
643	17	36	G3	VSS	644	P36	VSS
644	17	37	G2	DDR0DQSP[10]	645	P33	VSS
645	17	38	G1	DDR0DQSN[10]	646	P30	VSS
646	18	1	F38	DDR0DQ[54]	647	P26	VSS
647	18	2	F37	DDR0DQ[55]	648	P23	VSS
648	18	3	F36	VSS	649	P16	VSS
649	18	4	F35	DDR0DQSN[7]	650	P12	VSS
650	18	5	F34	DDR0DQSP[7]	651	P11	VSS
651	18	6	F33	VSS	652	P10	VSS
652	18	7	F32	DDR1DQ[62]	653	P9	VSS
653	18	8	F31	DDR1DQ[58]	654	P8	VSS
654	18	9	F30	VSS	655	P7	VSS
655	18	10	F29	VSS	656	P6	VSS
656	18	11	F28	VSS	657	P3	VSS
657	18	12	F27	VSS	658	N36	VSS
658	18	13	F26	VSS	659	N33	VSS
659	18	14	F25	VSS	660	N30	VSS
660	18	15	F24	VSS	661	N29	VSS
661	18	16	F23	VSS	662	N28	VSS
662	18	17	F22	VSS	663	N27	VSS
663	18	18	F21	VSS	664	N23	VSS
664	18	19	F20	VMSEDQSP[4]	665	N16	VSS
665	18	20	F19	VSS	666	N12	VSS
666	18	21	F18	VSS	667	N9	VSS
667	18	22	F17	VSS	668	N6	VSS
668	18	23	F16	VSS	669	N3	VSS
669	18	24	F15	VSS	670	M36	VSS
670	18	25	F14	VMSEDQSP[3]	671	M33	VSS
671	18	26	F13	VSS	672	M30	VSS
672	18	27	F12	VSS	673	M27	VSS

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 18 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
673	18	28	F11	VSS	674	M25	VSS
674	18	29	F10	VSS	675	M24	VSS
675	18	30	F9	VSS	676	M23	VSS
676	18	31	F8	VMSEDQSP[1]	677	M21	VSS
677	18	32	F7	VSS	678	M20	VSS
678	18	33	F6	VSS	679	M19	VSS
679	18	34	F5	VSS	680	M18	VSS
680	18	35	F4	DDR0DQSN[9]	681	M16	VSS
681	18	36	F3	VSS	682	M12	VSS
682	18	37	F2	DDR0DQ[8]	683	M9	VSS
683	18	38	F1	DDR0DQ[9]	684	M6	VSS
684	19	1	E38	VSS	685	M3	VSS
685	19	2	E37	DDR0DQ[50]	686	L38	VSS
686	19	3	E36	VSS	687	L37	VSS
687	19	4	E35	DDR0DQ[62]	688	L36	VSS
688	19	5	E34	DDR0DQ[58]	689	L33	VSS
689	19	6	E33	VSS	690	L32	VSS
690	19	7	E32	DDR1DQ[63]	691	L31	VSS
691	19	8	E31	DDR1DQ[59]	692	L30	VSS
692	19	9	E30	VSS	693	L27	VSS
693	19	10	E29	VMSEDQ[51]	694	L23	VSS
694	19	11	E28	VMSEDQ[54]	695	L16	VSS
695	19	12	E27	VMSEDQSN[6]	696	L12	VSS
696	19	13	E26	VSS	697	L9	VSS
697	19	14	E25	VMSEDQ[53]	698	L6	VSS
698	19	15	E24	VMSEDQ[48]	699	L3	VSS
699	19	16	E23	VSS	700	L2	VSS
700	19	17	E22	VMSEDQ[35]	701	L1	VSS
701	19	18	E21	VMSEDQ[38]	702	K36	VSS
702	19	19	E20	VMSEDQSN[4]	703	K35	VSS
703	19	20	E19	VMSEDQ[37]	704	K34	VSS
704	19	21	E18	VMSEDQ[32]	705	K33	VSS
705	19	22	E17	VSS	706	K30	VSS
706	19	23	E16	VMSEDQ[27]	707	K27	VSS
707	19	24	E15	VMSEDQ[30]	708	K25	VSS
708	19	25	E14	VMSEDQSN[3]	709	K23	VSS
709	19	26	E13	VMSEDQ[29]	710	K16	VSS
710	19	27	E12	VMSEDQ[24]	711	K12	VSS
711	19	28	E11	VSS	712	K9	VSS
712	19	29	E10	VMSEDQ[11]	713	K6	VSS
713	19	30	E9	VMSEDQ[14]	714	K5	VSS

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 19 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
714	19	31	E8	VMSEDQSN[1]	715	K4	VSS
715	19	32	E7	VMSEDQ[13]	716	K3	VSS
716	19	33	E6	VMSEDQ[8]	717	J36	VSS
717	19	34	E5	VSS	718	J33	VSS
718	19	35	E4	DDR0DQSP[9]	719	J30	VSS
719	19	36	E3	VSS	720	J27	VSS
720	19	37	E2	DDR0DQ[13]	721	J26	VSS
721	19	38	E1	VSS	722	J23	VSS
722	20	1	D38	VSS	723	J22	VSS
723	20	2	D37	DDR0DQ[51]	724	J21	VSS
724	20	3	D36	VSS	725	J20	VSS
725	20	4	D35	DDR0DQ[63]	726	J19	VSS
726	20	5	D34	DDR0DQ[59]	727	J18	VSS
727	20	6	D33	VSS	728	J17	VSS
728	20	7	D32	VSS	729	J16	VSS
729	20	8	D31	VSS	730	J14	VSS
730	20	9	D30	VSS	731	J12	VSS
731	20	10	D29	VMSEDQ[50]	732	J9	VSS
732	20	11	D28	VMSEDQ[55]	733	J6	VSS
733	20	12	D27	VMSEDQSP[6]	734	J3	VSS
734	20	13	D26	VSS	735	H36	VSS
735	20	14	D25	VMSEDQ[49]	736	H33	VSS
736	20	15	D24	VMSEDQ[52]	737	H30	VSS
737	20	16	D23	VSS	738	H27	VSS
738	20	17	D22	VMSEDQ[34]	739	H24	VSS
739	20	18	D21	VMSEDQ[39]	740	H21	VSS
740	20	19	D20	VSS	741	H17	VSS
741	20	20	D19	VMSEDQ[33]	742	H12	VSS
742	20	21	D18	VMSEDQ[36]	743	H9	VSS
743	20	22	D17	VSS	744	H6	VSS
744	20	23	D16	VMSEDQ[26]	745	H3	VSS
745	20	24	D15	VMSEDQ[31]	746	G36	VSS
746	20	25	D14	VSS	747	G33	VSS
747	20	26	D13	VMSEDQ[25]	748	G30	VSS
748	20	27	D12	VMSEDQ[28]	749	G27	VSS
749	20	28	D11	VSS	750	G24	VSS
750	20	29	D10	VMSEDQ[10]	751	G21	VSS
751	20	30	D9	VMSEDQ[15]	752	G17	VSS
752	20	31	D8	VSS	753	G14	VSS
753	20	32	D7	VMSEDQ[9]	754	G9	VSS
754	20	33	D6	VMSEDQ[12]	755	G8	VSS

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 20 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
755	20	34	D5	VSS	756	G7	VSS
756	20	35	D4	DDR0DQ[1]	757	G6	VSS
757	20	36	D3	VSS	758	G3	VSS
758	20	37	D2	DDR0DQ[12]	759	F36	VSS
759	20	38	D1	VSS	760	F33	VSS
760	21	1	C38	VSS	761	F30	VSS
761	21	2	C37	VSS	762	F29	VSS
762	21	3	C36	VSS	763	F28	VSS
763	21	4	C35	VSS	764	F27	VSS
764	21	5	C34	VSS	765	F26	VSS
765	21	6	C33	VSS	766	F25	VSS
766	21	7	C32	VMSEDQSP[7]	767	F24	VSS
767	21	8	C31	VSS	768	F23	VSS
768	21	9	C30	VSS	769	F22	VSS
769	21	10	C29	VSS	770	F21	VSS
770	21	11	C28	VSS	771	F19	VSS
771	21	12	C27	VSS	772	F18	VSS
772	21	13	C26	VMSEDQSP[5]	773	F17	VSS
773	21	14	C25	VSS	774	F16	VSS
774	21	15	C24	VSS	775	F15	VSS
775	21	16	C23	VSS	776	F13	VSS
776	21	17	C22	VSS	777	F12	VSS
777	21	18	C21	VSS	778	F11	VSS
778	21	19	C20	VMSEDQSN[8]	779	F10	VSS
779	21	20	C19	VSS	780	F9	VSS
780	21	21	C18	VSS	781	F7	VSS
781	21	22	C17	VSS	782	F6	VSS
782	21	23	C16	VSS	783	F5	VSS
783	21	24	C15	VSS	784	F3	VSS
784	21	25	C14	VMSEDQSP[2]	785	E38	VSS
785	21	26	C13	VSS	786	E36	VSS
786	21	27	C12	VSS	787	E33	VSS
787	21	28	C11	VSS	788	E30	VSS
788	21	29	C10	VSS	789	E26	VSS
789	21	30	C9	VSS	790	E23	VSS
790	21	31	C8	VMSEDQSN[0]	791	E17	VSS
791	21	32	C7	VSS	792	E11	VSS
792	21	33	C6	VSS	793	E5	VSS
793	21	34	C5	VSS	794	E3	VSS
794	21	35	C4	DDR0DQ[5]	795	E1	VSS
795	21	36	C3	DDR0DQ[0]	796	D38	VSS

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 21 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
796	21	37	C2	VSS	797	D36	VSS
797	21	38	C1	VSS	798	D33	VSS
798	22	1	B38	VSS	799	D32	VSS
799	22	2	B37	VSS	800	D31	VSS
800	22	3	B36	VSS	801	D30	VSS
801	22	4	B35	VMSEDQ[59]	802	D26	VSS
802	22	5	B34	VMSEDQ[62]	803	D23	VSS
803	22	6	B33	VMSEDQ[58]	804	D20	VSS
804	22	7	B32	VMSEDQSN[7]	805	D17	VSS
805	22	8	B31	VMSEDQ[60]	806	D14	VSS
806	22	9	B30	VMSEDQ[56]	807	D11	VSS
807	22	10	B29	VSS	808	D8	VSS
808	22	11	B28	VMSEDQ[43]	809	D5	VSS
809	22	12	B27	VMSEDQ[42]	810	D3	VSS
810	22	13	B26	VMSEDQSN[5]	811	D1	VSS
811	22	14	B25	VMSEDQ[44]	812	C38	VSS
812	22	15	B24	VMSEDQ[40]	813	C37	VSS
813	22	16	B23	VSS	814	C36	VSS
814	22	17	B22	VMSEECC[3]	815	C35	VSS
815	22	18	B21	VMSEECC[2]	816	C34	VSS
816	22	19	B20	VMSEDQSP[8]	817	C33	VSS
817	22	20	B19	VMSEECC[4]	818	C31	VSS
818	22	21	B18	VMSEECC[0]	819	C30	VSS
819	22	22	B17	VSS	820	C29	VSS
820	22	23	B16	VMSEDQ[19]	821	C28	VSS
821	22	24	B15	VMSEDQ[18]	822	C27	VSS
822	22	25	B14	VMSEDQSN[2]	823	C25	VSS
823	22	26	B13	VMSEDQ[20]	824	C24	VSS
824	22	27	B12	VMSEDQ[16]	825	C23	VSS
825	22	28	B11	VSS	826	C22	VSS
826	22	29	B10	VMSEDQ[3]	827	C21	VSS
827	22	30	B9	VMSEDQ[2]	828	C19	VSS
828	22	31	B8	VMSEDQSP[0]	829	C18	VSS
829	22	32	B7	VMSEDQ[4]	830	C17	VSS
830	22	33	B6	VMSEDQ[0]	831	C16	VSS
831	22	34	B5	VSS	832	C15	VSS
832	22	35	B4	DDR0DQ[4]	833	C13	VSS
833	22	36	B3	VSS	834	C12	VSS
834	22	37	B2	VSS	835	C11	VSS
835	22	38	B1	----	836	C10	VSS
836	23	1	A38	----	837	C9	VSS

Table 2-4. Intel® C102/C104 Scalable Memory Buffer Ball List (Sheet 22 of 22)

	Row	Column	Ball #	Ball Name	Sort No.	Ball #	BALL NAME
837	23	2	A37	VSS	838	C7	VSS
838	23	3	A36	VSS	839	C6	VSS
839	23	4	A35	VSS	840	C5	VSS
840	23	5	A34	VSS	841	C2	VSS
841	23	6	A33	VMSEDQ[63]	842	C1	VSS
842	23	7	A32	VSS	843	B38	VSS
843	23	8	A31	VMSEDQ[57]	844	B37	VSS
844	23	9	A30	VMSEDQ[61]	845	B36	VSS
845	23	10	A29	VSS	846	B29	VSS
846	23	11	A28	VMSEDQ[46]	847	B23	VSS
847	23	12	A27	VMSEDQ[47]	848	B17	VSS
848	23	13	A26	VSS	849	B11	VSS
849	23	14	A25	VMSEDQ[41]	850	B5	VSS
850	23	15	A24	VMSEDQ[45]	851	B3	VSS
851	23	16	A23	VSS	852	B2	VSS
852	23	17	A22	VMSEECC[6]	853	A37	VSS
853	23	18	A21	VMSEECC[7]	854	A36	VSS
854	23	19	A20	VSS	855	A35	VSS
855	23	20	A19	VMSEECC[1]	856	A34	VSS
856	23	21	A18	VMSEECC[5]	857	A32	VSS
857	23	22	A17	VSS	858	A29	VSS
858	23	23	A16	VMSEDQ[22]	859	A26	VSS
859	23	24	A15	VMSEDQ[23]	860	A23	VSS
860	23	25	A14	VSS	861	A20	VSS
861	23	26	A13	VMSEDQ[17]	862	A17	VSS
862	23	27	A12	VMSEDQ[21]	863	A14	VSS
863	23	28	A11	VSS	864	A11	VSS
864	23	29	A10	VMSEDQ[6]	865	A8	VSS
865	23	30	A9	VMSEDQ[7]	866	A5	VSS
866	23	31	A8	VSS	867	A4	VSS
867	23	32	A7	VMSEDQ[1]	868	A3	VSS
868	23	33	A6	VMSEDQ[5]			
869	23	34	A5	VSS			
870	23	35	A4	VSS			
871	23	36	A3	VSS			
872	23	37	A2	----			
873	23	38	A1	----			

2.4 Intel® C102/C104 Scalable Memory Buffer Package Specifications

The Intel® C102 Scalable Memory Buffer is a bare die component surface mounted on FCBGA10 package form factor with a total of 868 lead-free solder balls in a grid array of 0.8 mm pitch on a 31 mm x 19.5 mm package body. Additional package mechanical specifications are documented in the *Intel® C102/C104 Scalable Memory Buffer Thermal Mechanical Specifications and Design Guide*.

§

3 Electrical and Power Specifications

3.1 Overview

This chapter contains a description of the Intel® C102/C104 Scalable Memory Buffer component's electrical DC parameters, timing parameters and power considerations.

3.2 Storage Conditions

Table 3-1 contains absolute maximum ratings over operating free-air temperature range (see Note 1).

Table 3-1. Storage Condition Ratings

Symbol	Parameter	Min	Max	Notes
$T_{absolute\ storage}$	The minimum/maximum non-operating device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-55°C	125°C	1, 2, 3
$T_{sustained\ storage}$	The minimum/maximum device in storage temperature (in shipping media) for a sustained period of time	-5°C	40°C	4, 5
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	-60% @ 24°		5, 6
$Time_{sustained\ storage}$	A prolonged or extended period of time; typically associated with customer shelf life	0 month	6 months	6

Notes:

1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified in by applicable JEDEC standard and MAS document. Non-adherence may affect component reliability.
3. $T_{absolute\ storage}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel® branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40°C to 70°C & Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28°C) Post board attach storage temperature limits are not specified for non-Intel® branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{sustained\ storage}$ and customer shelf life in applicable Intel box and bags.

3.3 Electrical DC Absolute Maximum Ratings

Table 3-2 contains absolute maximum ratings over operating free-air temperature range (see Note 1).

Table 3-2. Absolute Maximum Ratings Over Operating Free-Air Temperature Range[1] (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit
VCCADDRDLL_1P5 VCCAVMSEPLL_1P5 VCCAMISCTS_1P5	Voltage for DLL, PLL etc (1.5 V)	-0.4	1.89	V

Table 3-2. Absolute Maximum Ratings Over Operating Free-Air Temperature Range[1] (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit
VCCDCORE_1P0 VCCDVMSEIO_1P0	Both these rails come from the same VR. VCCDCORE_1P0 = Voltage for Intel® C102/C104 Scalable Memory Buffer Core. (1 V) VCCDVMSEIO_1P0 = VMSE analog circuits (1.0 V)	-0.4	1.08	V
VCCADDRIO_1P5 1.5/1.35 V	Voltage for DDR IO (1.5 V)	-0.4	1.89	V
VCCAVMSEIO_1P35	Voltage for VMSE IO (1.35 V)	-0.4	1.89	V

Notes:

1. Stresses beyond those listed under Table 3-2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Table 3-3" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.3.1 Intel® C102/C104 Scalable Memory Buffer Operating DC Parameters

Table 3-3 contains the electrical DC parameters for the Intel® C102/C104 Scalable Memory Buffer for normal operation. DC specifications are defined at the Intel® C102/C104 Scalable Memory Buffer pads, unless otherwise noted. DC specifications are only valid while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each specification. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.

Table 3-3. Intel® C102/C104 Scalable Memory Buffer Operating DC Electrical Parameters

Parameter	Min	Typ	Max	Units	Notes
VCCADDRDLL_1P5 VCCAVMSEPLL_1P5 VCCAMISCTS_1P5	1.384	1.5	1.58	V	1
VCCDCORE_1P0 VCCDVMSEIO_1P0	0.92	1.0	1.045	V	1
VCCADDRIO_1P5	1.463(@1.5) 1.312(@1.35)	1.515 (@1.5) 1.364(@1.35)	1.58(@1.5) 1.429(@1.35)	V	1
VCCAVMSEIO_1P35	1.312	1.35	1.42	V	1

Note:
1. the above specs are AC+DC, which includes the VR(DC+Ripple tolerance)

3.3.2 Intel® C102/C104 Scalable Memory Buffer Power Specifications

Table 3-4 contain the Intel® C102/C104 Scalable Memory Buffer maximum current specifications for the various rails. The minimum power supply ramp up rate is 5 mV/us.

Table 3-4. Intel® C102/C104 Scalable Memory Buffer Active Power Specifications

Parameter	Power Supply	Max Current	Units
VCCADDRDLL_1P5 VCCAVMSEPLL_1P5 VCCAMISCTS_1P5	@1.5 V	1	A
VCCDCORE_1P0 VCCDVMSEIO_1P0	@1.0 V	4	A
VCCADDRIO_1P5 1.5/1.35/	@1.5/1.35 V	2	A
VCCAVMSEIO_1P35	@1.35 V	1	A

3.4 DC Specifications

DC specifications are specified at Intel® C102/C104 Scalable Memory Buffer pads i.e. package pins, unless otherwise noted.

3.4.1 Intel® SMI 2 Signal DC Specifications

Contact your local Intel sales office or your distributor to obtain the Intel® SMI 2 specifications.

3.4.2 DDR3 Signal DC Specifications

In Table 3-5, **VCCD refers to the VCCADDRIO_1P5 voltage rail.**

Table 3-5. DDR3 and DDR3L Signal DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
I_{IL}	Input Leakage Current	-500		+500	uA	10
Data Signals						
V_{IL}	Input Low Voltage			$0.43*V_{CCD}$	V	2, 3
V_{IH}	Input High Voltage	$0.57*V_{CCD}$			V	2, 4, 5
R_{ON}	DDR3 Data Buffer On Resistance	21		31	Ω	6
Data ODT	On-Die Termination for Data Signals	45 90		55 110	Ω	8
PAR_ERR_N ODT	On-Die Termination for Parity Error Signals	59		72	Ω	
Reference Clock Signals, Command, and Data Signals						
V_{OL}	Output Low Voltage		$(V_{CCD} / 2)* (R_{ON} / (R_{ON}+R_{VTT\_TERM}))$		V	2, 7
V_{OH}	Output High Voltage		$V_{CCD} - ((V_{CCD} / 2)* (R_{ON}/ (R_{ON}+R_{VTT\_TERM}))$		V	2, 5, 7
Reference Clock Signal						

Table 3-5. DDR3 and DDR3L Signal DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
R_{ON}	DDR3 Clock Buffer On Resistance	21		31	Ω	6
Command Signals						
R_{ON}	DDR3 Command Buffer On Resistance	16		24	Ω	6
R_{ON}	DDR3 Reset Buffer On Resistance	25		75	Ω	6
$V_{OL\_CMOS1.5v}$	Output Low Voltage, Signals DDR{0/1}RESET_N			0.2*V_{CCD}	V	1,2
$V_{OH\_CMOS1.5v}$	Output High Voltage, Signals DDR{0/1}RESET_N	0.9*V_{CCD}			V	1,2
$I_{IL\_CMOS1.5v}$	Input Leakage Current	-100		+100	µA	1,2
Control Signals						
R_{ON}	DDR3 Control Buffer On Resistance	21		31	Ω	6
DDR_RCOMP	COMP Resistance	99	100	101	Ω	9

Notes:
1. Unless otherwise noted, all specifications in this table apply to all Intel® C102/C104 Scalable Memory Buffer frequencies.
2. The voltage rail V_{CCD} which will be set to 1.50 V or 1.35 V nominal depending on the voltage of all DIMMs connected to the processor.
3. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CCD}. However, input signal drivers must comply with the signal quality specifications.
6. This is the pull down driver resistance. Refer to processor signal integrity models for I/V characteristics. Reset drive does not have a termination.
7. R_{VTT_TERM} is the termination on the DIMM and not controlled by the Intel® C102/C104 Scalable Memory Buffer. Please refer to the applicable DIMM data sheet.
8. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
9. COMP resistance must be provided on the system board with 1% resistors. DDR_RCOMP resistors are terminated to VSS.
10. Input leakage current is specified for all DDR3 signals.

3.4.3 SMbus DC Specifications

Table 3-6. SMBus DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.3*V_{TT}	V	VTT= VCCDCORE_1P0
V_{IH}	Input High Voltage	0.7*VTT		V	
V_{OL}	Output Low Voltage		0.2*V_{TT}	V	
V_{OH}	Output High Voltage		$V_{TT(max)}$	V	
R_{ON}	Buffer On Resistance		44	Ω	
I_L	Leakage Current	-100	+100	µA	

3.4.4 JTAG DC Specifications

Table 3-7. JTAG Signals DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.3*V_{TT}	V	VTT= VCCDCORE_1P0

Table 3-7. JTAG Signals DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
V_{IH}	Input High Voltage	0.7*V_{TT}		V	
V_{OL}	Output Low Voltage (R_{TEST} = 500 ohm)		0.12*V_{TT}	V	
V_{OH}	Output High Voltage (R_{TEST} = 500 ohm)	0.88*V_{TT}		V	
R_{ON}	Buffer On Resistance Signals TDO	5	18	Ω	
I_{IL}	Input Leakage Current Signals TCK, TDI, TMS, TRST_N	-50	+50	µA	
I_{IL}	Input Leakage Current Signals TDO (R_{TEST} = 50 ohm)	-900	+900	µA	
I_O	Output Current (R_{TEST} = 500 ohm)	-1.50	+1.50	mA	
	Input Edge Rate Signals: TCK, TDI, TMS, TRST_N	0.5		V/ns	These are measured between VIL and VIH.

3.4.5 Misc Signals

Table 3-8. VCCPWRGOOD, VDDPWRGOOD and RST_N AC and DC Characteristics

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage	0.75*vccdcore_1p0		V
V_{IL}	Input Low voltage		0.15*vccdcore_1p0	V
V_{HYST}	Hysteresis Voltage	300	600	mV
t_R	PWRGOOD Rise Time	10	100000	ns
t_F	PWRGOOD Fall Time	10	100000	ns
$I_{LEAK-PIN}$	Input Leakage per device pin	-20	20	uA
C_{PADI}	I/O Pin Capacitance		7	pF

Table 3-9. REFCLK Specification

Symbol	Value	Unit	Note
Vref	0.5*vccdvmseio_1p0	V	
Vih	0.75*vref	V	
Vil	0.25*vref	V	
Slew Rate	20% to 80% 0.38 ns ±0.12 ns	ns	
Frequency	100	MHz	Need to support Spread Spectrum Clocking, down to -0.5% of the operating frequency, with modulation frequency of 30 to 33KHz.

3.5 Cold Power Up Sequence

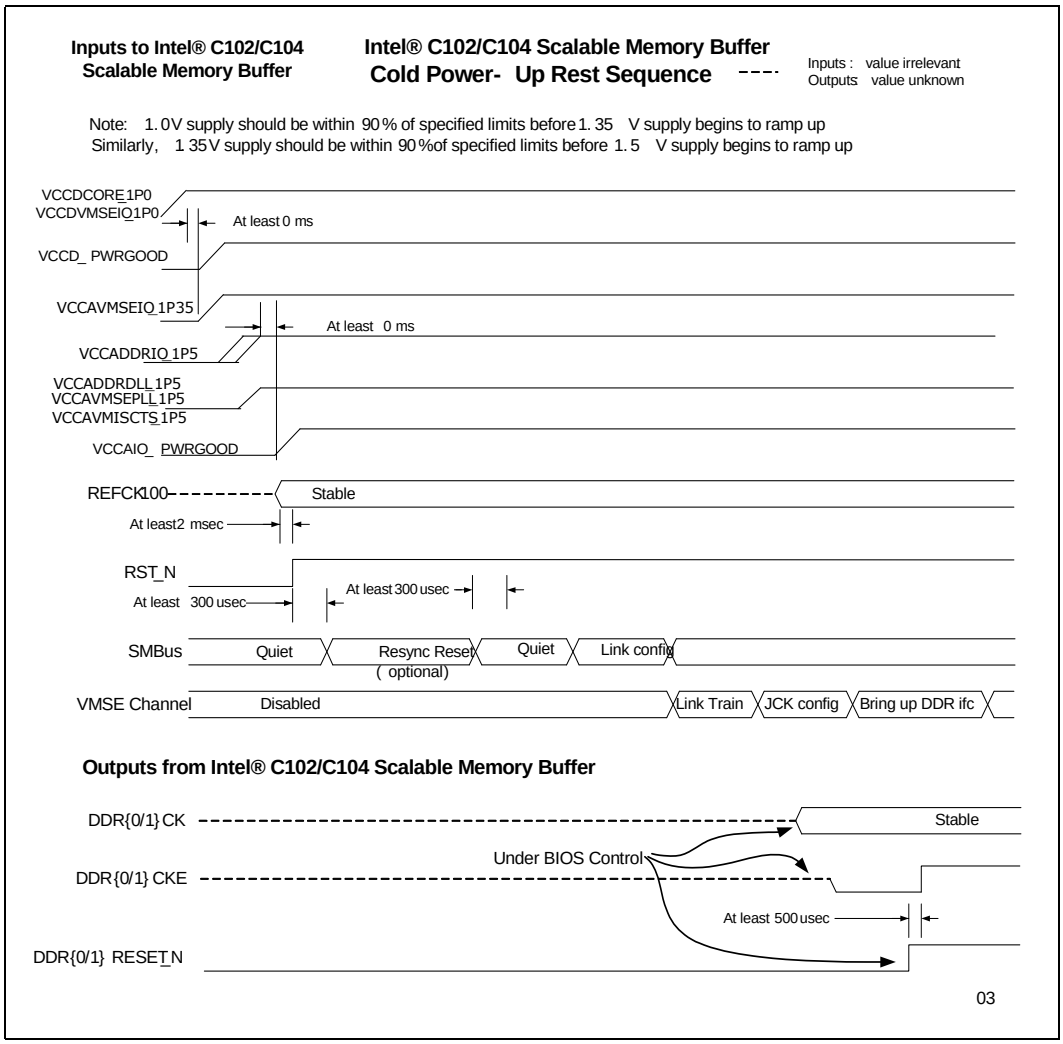
The timing diagram shown in figure 10-1 represents the power up sequence to be followed for all the power rails to Intel® C102/C104 Scalable Memory Buffer.

Note: VCCD_PWRGOOD can be delayed to assert at the same time as VCCAIO_PWRGOOD, as long as all supplies are valid.

VCCADDRIO_1P5 can power up before or at the same time as VCCADDRDLL_1P5/ VCCAVMSEPLL_1P5/VCCAMISCTS_1P5 rail. The Intel reference platform implementation powers up the VCCADDRIO_1P5 rail before the VCCADDRDLL_1P5 rail.

During power down, after asserting RST_N all the supplies can be powered down including the two PWRGOOD signals.

Figure 3-1. Intel® C102/C104 Scalable Memory Buffer Cold Power-Up Reset Sequence



3.6 DDR3 Signal Quality Specifications

Various scenarios for the DDR3 Signals have been simulated to generate a set of layout guidelines which are available in the *Platform Design Guide (PDG)*.

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below VSS. The overshoot/undershoot specifications limit transitions beyond specified maximum voltages or VSS due to the fast signal edge rates. Intel® C102/C104 Scalable Memory Buffer can be damaged by single and/or repeated overshoot or

undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in Table 3-10 will insure reliable IO performance for the lifetime of the Intel® C102/C104 Scalable Memory Buffer.

3.6.0.1 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to V_{SS}. It is important to note that the overshoot and undershoot conditions are separate and their impact must be determined independently.

The pulse magnitude and duration must be used to determine if the overshoot/undershoot pulse is within specifications.

3.6.0.2 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

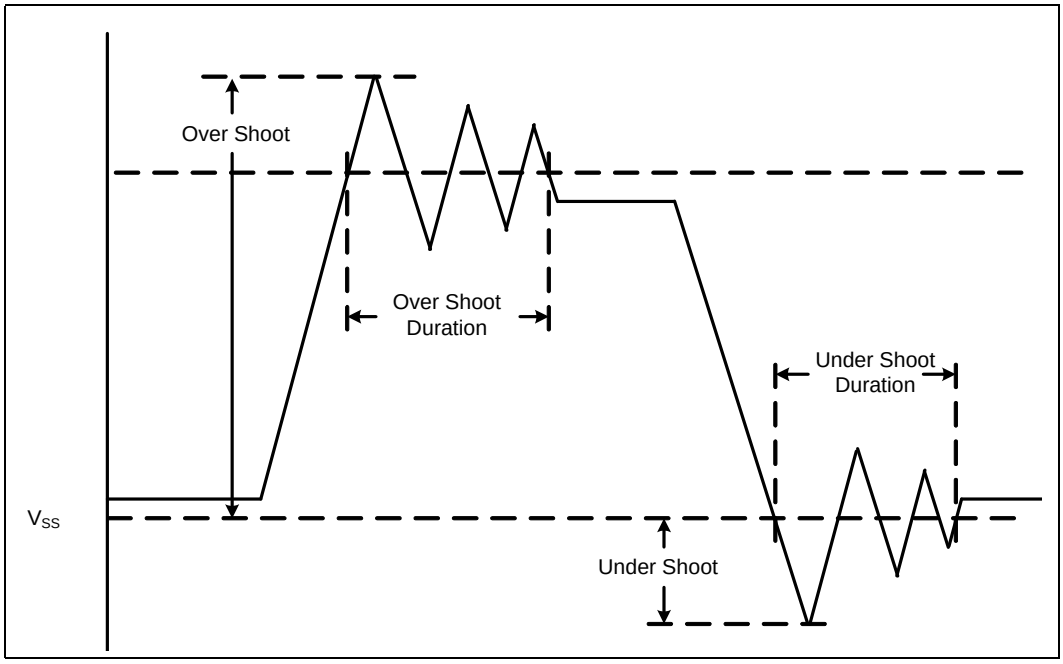
Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Table 3-10. DDR3 I/O Overshoot/Undershoot Specifications

Signal Group	Minimum Undershoot	Maximum Overshoot	Overshoot Duration	Undershoot Duration	Notes
DDR3	-0.2 * V_{CCD}	1.2 * V_{CCD}	0.25*T_{CH}	0.1*T_{CH}	1,2,3

Notes:
1. These specifications are measured at the Intel® C102/C104 Scalable Memory Buffer pad. VCCD refers to the VCCADDRIO_1P5 voltage rail.
2. Refer to Figure 3-2 for description of allowable Overshoot/Undershoot magnitude and duration.
3. T_{CH} is the minimum high pulse width duration, see Table 3-5 for details on DDR3 T_{CH}.

Figure 3-2. Maximum Acceptable Overshoot/Undershoot Waveform



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4 Configuration Registers

This section documents a subset of the CSRs supported by Intel® C102/C104 Scalable Memory Buffer component. The CSRs pertain to device identification and error status of the Intel® C102/C104 Scalable Memory Buffer component.

4.1 Register Attributes

All registers have a Base Attribute, as defined in Table 4-1. Some register attributes are further modified with Attribute Modifiers, as defined in Table 4-2.

Table 4-1. Register Base Attributes Definitions

Attribute	Abbreviation	Description
Read Only	RO	These bits can only be read by software, writes have no effect. The value of the bits is determined by the hardware only.
Read/Write	RW	The bit can be read or written by software.
Read/Write 1 to Clear	RW1C	The bit can be either read or cleared by software. In order to clear a bit, the software must write a one to it. Writing a zero to an RW1C bit will have no effect. Hardware will set this bit.
Reserved	RV	These bits are reserved for future expansion and may be defined in future revisions of this specification. For forward compatibility, their value must not be modified by software. When writing these bits, software must preserve the value read. For the component that corresponds to this revision of the specification, the bits will return '0' when read.

Table 4-2. Register Attribute Modifier Definitions

Attribute Modifier	Abbreviation	Description
Sticky	S	The bit is "sticky" or unchanged by a VMSE Soft Reset command. These bits will return to a default state on assertion of the RST_N input pin.
Once	-O	After power-up reset, these bits can only be written by software once, after which the bits becomes "Read Only", until the next assertion of the RST_N input pin.
Variant	-V	The value of these bits can be updated by hardware

- The "S" modifier is appended to the end of the Base Attribute for compatibility with industry specs
- Modifiers with a leading '-' are appended (in alphabetical order) after a single '-' when more than one apply

4.1.1 Register Attribute Examples

- RO-V: Read Only Variant: Typically status bits
- ROS-V: Read Only Sticky Variant: Typically status bits
- RW-O: Read Write Once: Typically "static" capability or control bits that BIOS writes.
- RW-V: Read Write Variant: Commonly control bits that HW clears
- RWS: Read Write Sticky: Persistent control bits

- RW1CS: Read Write 1 to Clear Sticky: Error status bits

4.1.2 Register Addressing

In some cases, a single register definition is used for multiple instantiations of a register. In these cases, the register definition contains multiple offsets. For a register with a single range, offsets are listed left to right, in the same order as the register range. For example:

```
LOGWECC[1:0]
Offset: 228h, 224h
```

is read as:

- LOGWECC[1] = 228h
- LOGWECC[0] = 224h

For registers with multiple ranges the ranges are nested; the left-most range is the outer loop. For example:

```
LOGVCRC[1:0][1:0]
Offset: 220h, 21Ch, 218h, 214h
```

is read as:

- LOGVCRC[1][1] = 220h
- LOGVCRC[1][0] = 21Ch
- LOGVCRC[0][1] = 218h
- LOGVCRC[0][0] = 214h

4.1.3 Number Notations

References in this specification are made to non-zero numbers in binary, decimal, and hexadecimal formats using the following notations. References to zero or one may be made in any of the following formats, or also unambiguously as '0' or '1'.

Table 4-3. Number Notations

Base	Notation	Description	Example
binary	XXb	XX=binary value	010b
decimal	XXd	XX=decimal value	31d
hexadecimal	XXh	XX=hexadecimal value	FFDE_1234h

4.2 Intel® C102/C104 Scalable Memory Buffer Memory Buffer Register Descriptions

4.2.1 PCI Express* Configuration Header

To assist in System Address Mapping, discovery and identification, Intel® C102/C104 Scalable Memory Buffer includes a PCI Express configuration space header, located in the address ranges 00h-7Ah, and 100h-103h. All registers within the address ranges 00h-7Ah that are not defined below will respond as unimplemented registers - writes will have no effect and reads will return zeros.

4.2.1.1 VID: Vendor ID

VID Offset: 000h			
Bits	**Attr**	**Default**	**Description**
15:0	RO	8086h	VID: This value is assigned by PCI-SIG to Intel.

4.2.1.2 DID: Device ID

DID Offset: 002h			
Bits	**Attr**	**Default**	**Description**
15:0	RO	0883h	DID: 0883h: This value is assigned by Intel to Intel® C102/C104 Scalable Memory Buffer.

4.2.1.3 PCISTS: Status

PCISTS Offset: 006h			
Bits	**Attr**	**Default**	**Description**
15:5	RV	0	Reserved
4	RO	1b	Capabilities_List: This bit indicates the presence of a capabilities list structure
3:0	RV	0	Reserved

4.2.1.4 RID: Revision ID

This Register contains the revision number of Intel® C102/C104 Scalable Memory Buffer.

RID Offset: 008h			
Bits	**Attr**	**Default**	**Description**
7:0	RO-V	21h	21h = C1 stepping

4.2.1.5 CCR: Class Code Register

CCR Offset: 009h			
Bits	**Attr**	**Default**	**Description**
23:16	RO	08h	Base_Class: Generic Device.
15:8	RO	80h	Sub_Class: Generic Device.
7:0	RO	00h	Reg_Lev_Prog_Int: Set to 00h for all non-APIC devices

4.2.1.6 CLSR: Cache Line Size Register

CLSR Offset: 00Ch			
Bits	**Attr**	**Default**	**Description**
7:0	RW	00h	CLSR: This register is set as RW for compatibility reasons only.

4.2.1.7 HDR: Header Type Register

HDR Offset: 00Eh			
Bits	**Attr**	**Default**	**Description**
7	RW-O	0	Mult_Func_Dev: BIOS can write this bit once at power up, depending on whether Intel® C102/C104 Scalable Memory Buffer will be mapped as a multi-function device or not, after which the bit becomes "Read Only", until the next assertion of the RST_N input pin. '0' = Single Function Device '1' = Multi-function Device
6:0	RV	0	Reserved

4.2.1.8 SVID: Subsytem Vendor ID

SVID Offset: 02Ch			
Bits	**Attr**	**Default**	**Description**
15:0	RW-O	8086h	SVID: The default value specifies Intel but can be set to any value once after reset, after which the bits become "Read Only", until the next assertion of the RST_N input pin.

Note: A single Configuration Write command should be used to write both bytes of this register at the same time. Intel® C102/C104 Scalable Memory Buffer may implement the write-once functionality on a byte-by-byte basis.

4.2.1.9 SDID: Subsytem Device ID

SDID Offset: 02Eh			
Bits	**Attr**	**Default**	**Description**
15:0	RW-O	0	SDID: Assigned by the subsystem vendor to uniquely identify the subsystem.

Note: A single Configuration Write command should be used to write both bytes of this register at the same time. Intel® C102/C104 Scalable Memory Buffer may implement the write-once functionality on a byte-by-byte basis.

4.2.1.10 CAPPTR: Capabilities Pointer

CAPPTR Offset: 034h			
Bits	**Attr**	**Default**	**Description**
7:0	RO	40h	CAPPTR: Points to the first capability structure for the device which is the PCIe capability.

4.2.1.11 PCPCAP: PCI Express Capabilities Structure

PCPCAP Offset: 040h			
Bits	**Attr**	**Default**	**Description**
31:24	RV	0	Reserved
23:20	RO	9h	DEVICETYPE: Device type is Root Complex Integrated Endpoint.
19:16	RO	1h	CAPABILITY_VERSION: PCI Express Capability is Compliant with Version 1.0 of the PCI Express Spec. ***Note:*** This capability structure is not compliant with Versions beyond 1.0.
15:8	RO	00h	NEXT_PTR:Pointer to the next capability. Set to 0 to indicate there are no more capability structures.
7:0	RO	10h	Capability_ID: Provides the PCI Express capability ID assigned by PCI-SIG.

4.2.1.12 PXPENHCAP:PCI Express Enhanced Capability Header

There are no enhanced capability structures in the enhanced configuration space. This register is reserved with zeros to prevent software from expecting further capability structures.

PXPENHCAP Offset: 100h			
Bits	**Attr**	**Default**	**Description**
31:0	RO	0	Reserved

4.2.1.13 TEMP: Temperature Register

This CSR indicates the present Intel® C102/C104 Scalable Memory Buffer temperature reading.

The Host memory controller reads the TEMP CSR for memory sub-system thermal management purposes.

TEMP Offset: 0AAh			
Bits	**Attr**	**Default**	**Description**
15:13	RV	0	Reserved

TEMP Offset: 0AAh			
Bits	**Attr**	**Default**	**Description**
12:2	RO-V	0	TEMPERATURE: 10-bit + sign data for the internal temperature measurement with 0.25°C resolution.
1:0	RV	0	Reserved

in order to match the encoding for LR DIMM and RDIMM temperature sensors, this register stores values from -256 to 255 degrees C measured in 0.25 degree increments, though the practical resolution is 0.5 degrees. The lease significant bit of TEMPERATURE will always be zero.

Examples of valid settings and interpretation of temperature register bits:

Table 4-4. Temperature Coding Examples

Temperature Register Coding Examples		
B15~B0 (binary)	**Value**	**Units**
xxx00000001010xx	+2.5	°C
xxx00000000100xx	+1.00	°C
xxx00000000010xx	+0.5	°C
xxx00000000000xx	0	°C
xxx11111111110xx	-0.5	°C
xxx11111111100xx	-1.00	°C
xxx11111110100xx	-2.5	°C

4.2.1.14 VMSE_STATUS: VMSE Status Rtn Register

This register contains a copy of the status returned to the host.

This register specifies the source of the error that caused the most recent assertion of the VMSE_ERR_N signal.

VMSE_STATUS Offset: 104h			
Bits	**Attr**	**Default**	**Description**
31:8	RV	0	Reserved
7	RO-V	0	DDR_PARERR_SRE_B: Register Parity error Bus B A 1 indicates that a Register Parity error has occurred on DRAM bus B (DDR1) while the self refresh entry state machine was in operation This error will also set bit-3 of this register.
6	RO-V	0	DDR_PARERR_SRE A: Register Parity error Bus A A 1 indicates that a Register Parity error has occurred on DRAM bus A (DDR0) while the self refresh entry state machine was in operation This error will also set bit-2 of this register.
5	RV	0	Reserved
4	RO-V	0	SOFTWARE_ERROR: Software Error Bit This bit indicates that a Software Error was detected (ERR bit of the Power Management Command set to a 1)

VMSE_STATUS Offset: 104h			
Bits	**Attr**	**Default**	**Description**
3	RO-V	0	DDR_PARERR_B: Register Parity error Bus B A 1 indicates that a Register Parity error has occurred on DRAM bus B (DDR1).
2	RO-V	0	DDR_PARERR_A: Register Parity error Bus A A 1 indicates that a Register Parity error has occurred on DRAM bus A (DDR0).
1	RO-V	0	WR_ECC_ERR: Write Push ECC error A 1 indicates that a Write Push ECC error has been detected.
0	RO-V	0	CMD_CRC_ERR: CMD# CRC Error A 1 indicates that a CMD# bus CRC error has been detected.

4.2.2 Error Logging Registers

These registers log errors detected by Intel® C102/C104 Scalable Memory Buffer.

4.2.2.1 FERR: First Error Register

This register logs the first error detected by Intel® C102/C104 Scalable Memory Buffer. If multiple errors are detected during the same cycle, they will all be logged in this register. If this register does not contain all zeroes (that is, if any error is logged in this register), then errors detected by Intel® C102/C104 Scalable Memory Buffer will be logged in the NERR register. In the event that software attempts to clear a bit by writing a '1' to it in the same cycle that an error is detected by Intel® C102/C104 Scalable Memory Buffer, the bit will remain set, so that the error will not be lost.

FERR Offset: 200h			
Bits	**Attr**	**Default**	**Description**
31:12	RV	0	Reserved
31:12	RV	0	Reserved
31:12	RV	0	Reserved
31:12	RV	0	Reserved
11	RW1CS	0	SOFTWARE_ERROR: Software Error Bit
10	RW1CS	0	VMSE_CRC1_ERR:
9	RW1CS	0	VMSE_CRC0_ERR:
8	RW1CS	0	UNIMP_CFG_ERR: Unimplemented Configuration Register Access
7	RW1CS	0	READ_ECC_ERR:
6	RW1CS	0	INJ_ERR: Injected Error
5	RW1CS	0	CATRIP: Catastrophic Overtemp
4	RW1CS	0	DDR1_PAR_ERR:
3	RW1CS	0	DDR0_PAR_ERR:
2	RW1CS	0	VMSE_WECC_ERR:
1:0	RV	0	Reserved

4.2.2.2 NERR: Next Error Register

This register logs all errors after the first error detected by Intel® C102/C104 Scalable Memory Buffer. If the FERR register does not contain all zeroes (that is, if any error is logged in that register), then errors detected by Intel® C102/C104 Scalable Memory Buffer will be logged in this register. In the event that software attempts to clear a bit by writing a '1' to it in the same cycle that an error is detected by Intel® C102/C104 Scalable Memory Buffer, the bit will remain set, so that the error will not be lost. If an error cannot be logged in this register because the associated bit is already set, then the ERR_OVFL bit will be set.

NERR
Offset: 204h

Bits	Attr	Default	Description
31:12	RV	0	Reserved
11	RW1CS	0	SOFTWARE_ERROR: Software Error Bit
10	RW1CS	0	VMSE_CRC1_ERR:
9	RW1CS	0	VMSE_CRC0_ERR:
8	RW1CS	0	UNIMP_CFG_ERR: Unimplemented Configuration Register Access
7	RW1CS	0	READ_ECC_ERR:
6	RW1CS	0	INJ_ERR: Injected Error
5	RW1CS	0	CATRIP: Catastrophic Overtemp
4	RW1CS	0	DDR1_PAR_ERR:
3	RW1CS	0	DDR0_PAR_ERR:
2	RW1CS	0	VMSE_WECC_ERR:
1	RV	0	Reserved
0	RW1CS	0	ERR_OVFL: This is a status bit that will be set if an error is detected and the associated error bit is already set in this register, preventing individual logging of that error.

4.2.2.3 LERR: Last Error Register

This register logs the last error detected by Intel® C102/C104 Scalable Memory Buffer. If multiple errors are detected during the same cycle, they will all be logged in this register. Note that the error(s) logged in this register will also be logged in either the FERR or NERR register. Intel® C102/C104 Scalable Memory Buffer will overwrite the entire contents of this register upon detecting each error. For that reason, the bits are defined with an RWS-V attribute.

LERR
Offset: 208h

Bits	Attr	Default	Description
31:12	RV	0	Reserved
11	RWS-V	0	SOFTWARE_ERROR: Software Error Bit
10	RWS-V	0	VMSE_CRC1_ERR:
9	RWS-V	0	VMSE_CRC0_ERR:
8	RWS-V	0	UNIMP_CFG_ERR: Unimplemented Configuration Register Access
7	RWS-V	0	READ_ECC_ERR:
6	RWS-V	0	INJ_ERR: Injected Error

LERR Offset: 208h			
Bits	**Attr**	**Default**	**Description**
5	RWS-V	0	CATRIP: Catastrophic Overtemp
4	RWS-V	0	DDR1_PAR_ERR:
3	RWS-V	0	DDR0_PAR_ERR:
2	RWS-V	0	VMSE_WECC_ERR:
1:0	RV	0	Reserved

4.2.2.4 EMASK: Error Mask Register

This register individually masks error reporting and logging. A '0' in any field enables that error. A '1' in any field masks that error. If an error is masked in this register, the error will not be logged in the FERR or NERR register, and will not cause the VMSE_ERR_N signal to assert. Not all errors cause the VMSE_ERR_N signal to assert.

EMASK Offset: 20Ch			
Bits	**Attr**	**Default**	**Description**
31:12	RV	0	Reserved
11	RWS	1	SOFTWARE_ERROR:
10	RWS	1	VMSE_CRC1_ERR: ***Note:*** VMSE_CRC1_ERR and VMSE_CRC_0_ERR must both be set to the same value in EMASK.
9	RWS	1	VMSE_CRC0_ERR: ***Note:*** VMSE_CRC1_ERR and VMSE_CRC_0_ERR must both be set to the same value in EMASK.
8	RWS	1	UNIMP_CFG_ERR:
7	RWS	1	READ_ECC_ERR:
6	RWS	1	INJ_ERR:
5	RWS	0	CATRIP:
4	RWS	1	DDR1_PAR_ERR:
3	RWS	1	DDR0_PAR_ERR:
2	RWS	1	VMSE_WECC_ERR:
1:0	RV	0	Reserved

4.2.2.5 LOGDDRPARITY[1:0]: DDR Bus Parity Register Error Log

These registers log the specific DDR parity error inputs that caused the DDRPAR error to be flagged. The contents of this register are only valid when the associated DDRPAR error is logged in FERR or NERR register.

LOGDDRPARITY[1:0] Offset: 212h, 210h			
Bits	**Attr**	**Default**	**Description**
15:11	RV	0	Reserved
10:8	RWS	7h	MASK: DDR parity error mask 0: enables that error 1: masks/disables that error

LOGDDRPARITY[1:0] Offset: 212h, 210h			
Bits	**Attr**	**Default**	**Description**
7:3	RV	0	Reserved
2:0	RWS-V	0	DETECT: DDR parity error detected (active high)

4.2.2.6 LOGVCRC[1:0][1:0]: Intel® SMI 2 CRC Error Log

These registers contain the unscrambled, high-true Intel® SMI 2 command packet(s) associated with the Intel® SMI 2 CRC error(s) logged in the FERR or NERR register. The contents of these registers are only valid when the associated VMSE_CRC_ERR bit is set in the FERR or NERR register. If the VMSE_CRC_ERR bit is set in both the FERR and NERR register, then the contents of these register are associated with the error logged in the FERR register.

LOGVCRC0[1:0] are only valid when VMSE_CRC0_ERR bit is set in the FERR or NERR register. If the VMSE_CRC0_ERR bit is set in both the FERR and NERR register, then the contents of these register are associated with the error logged in the FERR register.

LOGVCRC1[1:0] are only valid when VMSE_CRC1_ERR bit is set in the FERR or NERR register. If the VMSE_CRC1_ERR bit is set in both the FERR and NERR register, then the contents of these register are associated with the error logged in the FERR register.

LOGVCRC[1:0]1 contain bits 33:17 of the Intel® SMI 2 command packet(s).

LOGVCRC[1:0]0 contain bits 16:0 of the Intel® SMI 2 command packet(s).

The contents of these registers depend on the Intel® SMI 2 operation mode (2:1 vs. 1:1). For 2:1 Independent Channel Mode, LOGVCRC0[1:0] captures CRC error information related to the "A" slot, while LOGVCRC1[1:0] captures CRC error information related to the "B" slot.

Although the Intel® SMI 2 CMD_N bus carries the command in a low true format, these register contain a high true version of the command. The command is captured in these registers after unscrambling.

LOGVCRC[1:0][1:0] Offset: 220h, 21Ch, 218h, 214h			
Bits	**Attr**	**Default**	**Description**
31:17	RV	0	Reserved
16:0	RWS-V	0	VCMD:

4.2.2.7 LOGWECC2: Intel® SMI 2 Write ECC Error Log

This register contains information associated with the VMSE_WECC_ERR logged in the FERR or NERR register. The contents of this register is only valid when the VMSE_WECC_ERR bit is set in the FERR or NERR register. If the VMSE_WECC_ERR bit is set in both the FERR and NERR register, then the contents of this register are associated with the error logged in the FERR register.

LOGWECC2 Offset: 22Ch			
Bits	**Attr**	**Default**	**Description**
31:10	RV	0	Reserved
9:8	RWS-V	0	ECCMODE: The ECC Mode sent on the WP bits.
7	RV	0	Reserved
6	RWS-V	0	CDWRD1: code-word1 If set, indicates that the second code-word failed
5	RWS-V	0	CDWRD0: code-word0 If set, indicates that the first code-word failed
4:0	RWS-V	0	WBUFF: The write buffer associated with the error.

4.2.2.8 LOGWECC[1:0]: Intel® SMI 2 Write ECC Error Log

These registers contain the write data ECC bits associated with the VMSE_WECC_ERR logged in the FERR or NERR register. The contents of these registers are only valid when the VMSE_WECC_ERR bit is set in the FERR or NERR register. If the VMSE_WECC_ERR bit is set in both the FERR and NERR register, then the contents of this register are associated with the error logged in the FERR register.

LOGWEEC1 contains write data ECC bits from the second code word of the failing cacheline.

LOGWEEC0 contains write data ECC bits from the first code word of the failing cacheline.

Note: Unscrambled data is logged in these registers. When operating in 1:1 Sub-Channel Lockstep Mode, unswizzled data is logged in these registers.

LOGWECC[1:0] Offset: 228h, 224h			
Bits	**Attr**	**Default**	**Description**
31:24	RWS-V	0	PTY1:PTY1 of the code-word
23:16	RWS-V	0	PTY0:PTY0 of the code-word
15:8	RWS-V	0	CRC1:CRC1 of the code-word
7:0	RWS-V	0	CRC0:CRC0 of the code-word

4.2.2.9 LOGCFGRW: Intel® SMI 2 Unimplemented Configuration Address Error Log

This register contains information associated with the UNIMP_CFG_ERR logged in the FERR or NERR register. The contents of this register is only valid when the UNIMP_CFG_ERR bit is set in the FERR or NERR register. If the UNIMP_CFG_ERR bit is set in both the FERR and NERR register, then the contents of this register are associated with the error logged in the FERR register.

LOGCFGRW Offset: 238h			
Bits	**Attr**	**Default**	**Description**
31:20	RV	0	Reserved

LOGCFGRW Offset: 238h			
Bits	**Attr**	**Default**	**Description**
19:16	RWS-V	0	BE: BE[3:0] Byte enables ***Note:*** These are only valid on a CFG Write.
15:2	RWS-V	0	CFG_ADDR: CFG addr bits 15:2. Bits 1:0 are always zero, and are not stored.
1	RV	0	Reserved
0	RWS-V	0	CFGWRITE: Config Read or Write. 0 = CFG Read 1 = CFG Write

4.2.2.10 LOGRECC: Read ECC Error Log

This register contains information associated with the most recent Read ECC Error logged in the FERR or NERR register. The contents of this register is only valid when the READ_ECC_ERR bit is set in the FERR or NERR register. If the READ_ECC_ERR bit is set in both the FERR and NERR register, then the contents of this register are associated with the error logged in the NERR register.

LOGRECC Offset: 244h			
Bits	**Attr**	**Default**	**Description**
31:23	RV	0	Reserved
22:7	RWS-V	0	COL_ADDR: Column Address
6:3	RWS-V	0	RANK: Logical Rank
2	RWS-V	0	CHN: DDR bus
1:0	RWS-V	0	ECC_MODE: ECC Mode.

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